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1TBulk eDRAM Using Gate-Induced Drain-Leakage (GIDL) Current for High Speed and Low Power applications

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Abstract

A Capacitorless 1T-eDRAM cell using gate-induced drain leakage (GIDL) current for write operation was demonstrated for the first time on 1T-Bulk. GIDL writing mechanism leads to 2 times lower power consumption compared to conventional impact ionization (II) write mechanism. The extrapolated write time is 6ns for Vds=1V.

Introduction

Many recent studies show that 1T-DRAM cells, based on the floating body effect are interesting solutions compared to the standard 1T/1C cell for eDRAM applications. The 1T-DRAM concept was demonstrated on different CMOS platforms: bulk silicon [1-2-3-4-5], PDSOI [6-7], FDSOI [8-9] and more recently Independent Double Gate [10-11]. Most of 1T-DRAM cells use II current for write operation regarding speed. The GIDL as write operation mechanism has been proposed for the first time on PDSOI by Yoshida [12]. This paper proposes for the first time GIDL evaluation on 1T-Bulk capacitorless eDRAM cell. All measurements presented here are carried out on device presented figure 1. Device architecture is optimised for GIDL mechanism with heavily doped extension and large gate drain overlap.

Write GIDL mechanism

The GIDL current originates from band to band tunneling of electrons and occurs in the gate drain overlap region during application of a negative gate and positive drain bias (Fig.2). At the same time, tunneling electrons flow to the drain, the generated holes are accumulated in the floating body region. Table 1 reports bias memory operations for GIDL and II write mechanisms. For this device we observe on figure 3 a higher memory effect amplitude for GIDL write, similar to already observed on optimised II device published in [2].

Drain and Gate bias impact with GIDL write

Impact of gate bias is illustrated on figure 4. Memory effect amplitude increases when gate bias increases. Figure 5 shows memory amplitude increase when drain bias increases. In both cases, write operation is favoured.

Power consumption

Consumption is evaluated in terms of current for the different memory operations. Table 2 compares power consumption between GIDL and II current.

For read condition, read current is more important for II than GIDL write mechanism.

For write operation, consumption is divided by 2 for GIDL. This reduction can be attributed to a difference in the drain current during "1" write operation for GIDL and II (Fig.6). During GIDL "1" write, the drain current is the same as substrate current whereas for II "1"write, the drain current is more important than the substrate current. Power consumption can be further reduced by applying lower drain bias without write time penalty (discussed later on §write speed).

For both cases, consumption during erase operation is very low, since in this case the transistor is not open.

Write speed

The write time τ is defined by (1):

$$Qmem = \int_0^{\tau} (Isub - Ileakage)dt \qquad (1)$$

Qmem is the charge brought by GIDL or II mechanism less the charge flowing through the junction during state 1 programming operation. Charge evaluation is based on model [4]. This model has been calibrated with II or GIDL current modeling based on [13] and junction leakages. Charges are stored in the depletion region (Wp) of each junction (source, drain, gate and N-buried) and for each junction are given by (2):

$$\left|\delta Q(Vb)\right| = qNaS\left|Wp_{eq} - Wp_{"1"/"0"}(Vb)\right| \qquad (2)$$

Table 2 shows that GIDL mechanism allows faster write operation compared to II. Indeed figure 6 shows that GIDL programming conditions substrate current (Isub) is 2 decades more important than for II. That explains a 5.6ns write time for GIDL compared to 300ns for II. Figure 7 shows the correlation between the write time and gate voltage required for write "1". Write operation speeds in the nanosecond range can be obtained by applying -1.8V to the gate at a drain voltage of 1.8V. For II, 2.3V are necessary to obtain 5ns write time with this non optimized device for II (Fig.8). Time required for GIDL write "1" becomes shorter as gate bias becomes more negatively larger (Fig.7). Indeed GIDL current increases as voltage difference between gate and drain increases. Substrate potential (Vb) follows gate voltage because body is electrically floating. As a result, band-to-band tunneling current increases in accordance with large lateral electric field between body and drain (Fig.9) On the contrary to II, GIDL write time does not depend on longitudinal electric field (Fig.7). A lowest drain bias can be used without penalty on write time while maintaining the memory window.

Using GIDL mechanism for 1T-Bulk "1" write operation is also indicated for high speed and low power applications.

Retention

Figure 10 shows that retention is not affected by write mechanism. Mechanisms involved in data loss are intrinsic to the junctions. It depends on doping profile and quality of junctions [5]. 10ms are measured for both programming mechanisms at 21°C. This value is in range with standard 1T/1C eDRAM characteristics.

Gate length scaling

Table 3 reports the memory operation bias for (Lg = 176 nm) 50Å gate oxide device. Figure 11 shows similar memory effect amplitude for 33Å gate oxide device than for 50Å gate oxide device. Gate scaling does not impact memory effect amplitude with GIDL programming operation as lateral electric field is similar for both devices.

Moreover, write speed is not affected by gate oxide reduction. Figure 6 shows that substrate current is similar for 33Å and 50Å device for GIDL conditions again lateral electric field is similar for both devices.

Nevertheless, scaling the gate length, drain current increases, and consequently read consumption will increase without affecting write consumption.

Conclusion

We have demonstrated that using GIDL mechanism for write operation on 1T-Bulk eDRAM leads to similar write time and memory amplitude obtained on optimised device for II. Main advantage of GIDL is a low write drain current leading to a low power write consumption. 1T-Bulk using GIDL current should be a very promising embedded memory for low power and high-speed systems on chip.

Reference

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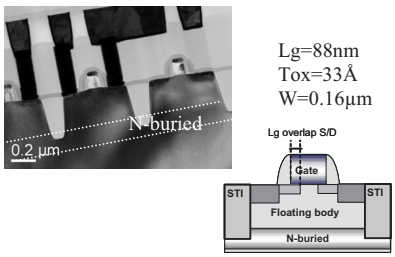

Fig.1: Cross section view of device fabricated with 90 nm technology in matrix environment and schematic view of 1T-bulk eDRAM with gate drain overlap region

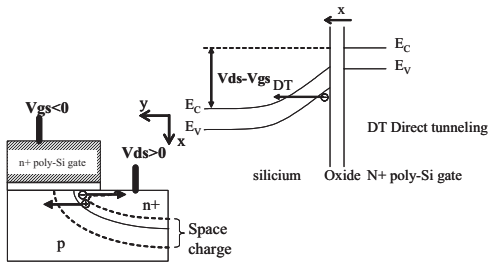

Fig.2: GIDL current is caused by band to band tunneling in the gate drain overlap region

	II Write	GIDL Write	Erase	Read	Hold
Vds (V)	+1.8	1.8	-1.2	+0.4	0
Vgs (V)	+1	-1.8	-1.2	+1	0
Vs (V)	0	0	0	0	0
$V_{N\text{-buried}}$ (V)	+0.6	+0.6	+0.6	+0.6	+0.6

Tab.1: Memory operating voltage conditions. All conditions have been chosen to reduce the number of voltage sources

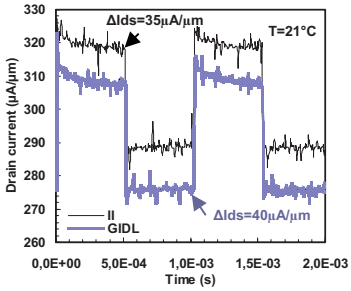

Fig.3: Read current margin between state 1 and state 0 for GIDL and II

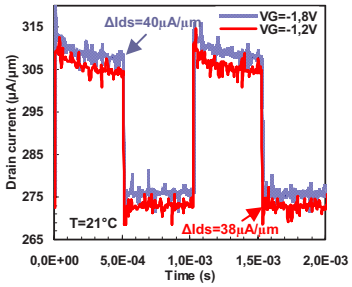

Fig.4: Drain current shift for different GIDL write gate bias

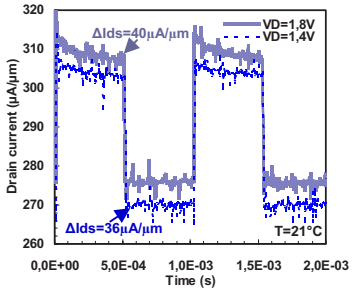

Fig.5: Drain current shift for different GIDL write drain bias

	Read			
	Vds [V]	Ids [µA]	P [mW]	Write time [ns]
II	0.4	49	0.0198	
GIDL	0.4	47	0.0188	
	Write			
II	1.8	104	0.187	300
GIDL	1.8	43	0.078	5.6

Tab.2: Write consumption and write time evaluation for GIDL and II

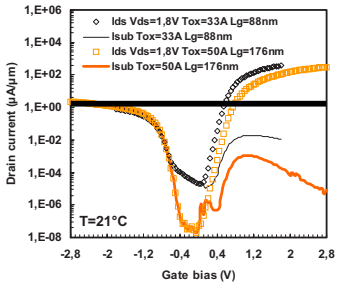

Fig.6: Predominance of GIDL and II current according gate bias. Measurements realised on similar devices without N-buried implant

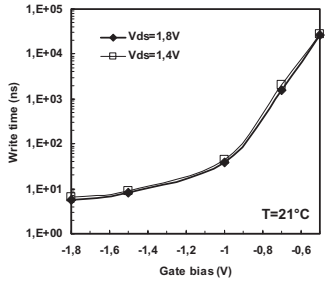

Fig.7: GIDL write time according bias for different drain bias

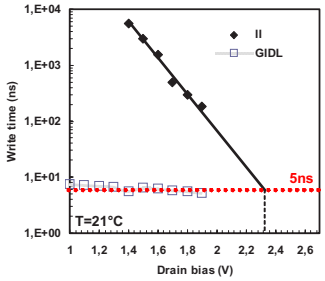

Fig.8: Write time for GIDL (V_G=-1.8V) and II (V_G=1V)

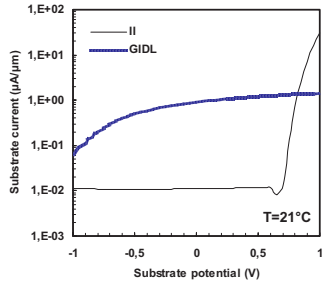

Fig.9: Visualisation of substrate current for II and GIDL according substrate potential

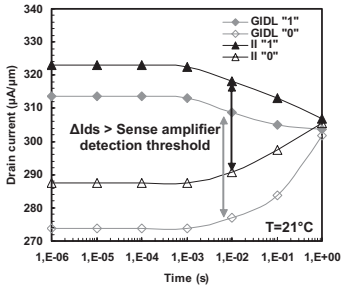

Fig.10: Retention characteristics show a retention time over 10ms at 21°C

	GIDL Write	Erase	Read	Hold
Vds (V)	2.5	-1.2	+0.4	0
Vgs (V)	-2.5	-1.2	+1.2	0
Vs (V)	0	0	0V	0
$V_{N\text{-buried}}$ (V)	+0.6	+0.6	+0.6	+0.6

Tab.3: Memory operating voltage conditions for Tox=50Å, Lg=176nm device

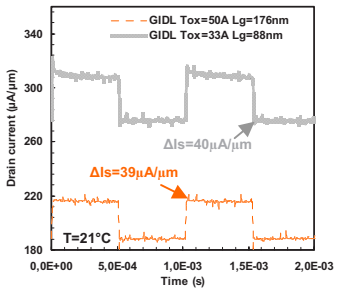

Fig.11: Read current margin for two devices Tox=33Å, Lg=88nm and Tox=50Å, Lg=176nm for bias presented respectively in Tab.1 and Tab.3