J-1-4

A Novel Multi-Fin DRAM Periphery Transistor Technology Using a Spacer Transfer through Gate Polysilicon Technique

Makoto Yoshida, Keunnam Kim, Jaerok Kahng, Chul Lee, Hyunju Sung, Kyoung-Ho Jung, Joon-Seok Moon, Wouns Yang and Kyung-Seok Oh

Advanced Technology Development Team 1, Semiconductor R&D Center, Samsung Electronics Co.,
San #16, Banwol-Dong, Hwasung-City, Kyunggi-Do, 445-701, KOREA
TEL +82-31-208-7959, FAX +82-31-208-4799, E-mail yoshida@samsung.com

Abstract

A new technique which integrates the metal gate multi-FinFETs and the conventional polysilicon gate planar FETs is proposed. It solves the problems of conventional scheme, such as complication of process integration due to coexistence of TiN gate FinFETs and polysilicon gate planar FETs, fin width consumption by multi gate oxidation, large fin-pitch limited by lithography and STI gap-filling. A newly proposed technique forms multi-fin structure by spacer transfer process through gate polysilicon electrode of planar FETs. Drain current gain due to increase of effective channel width is estimated and basic electrical characteristics of multi-FinFET are evaluated.

1. Introduction

It is expected that a half pitch of a DRAM memory cell will be shrunk by around 10% every year according to ITRS 2007. A cell size factor (which equals cell size divided by F^2, where F eqauls half pitch of a memory cell) will be also announced to be shrunk from 8 to 4 by 2011 to maintain competitiveness (Fig. 1)[1,2]. Dimension of the sense-amplifier and the sub-word driver (hereafter cell periphery) adjacent to the unit block of memory cells should be also shrunk to match small pitches of bit lines and word lines, respectively. Reduction of the cell periphery area size is also necessary to reduce a chip size, reduce an unnecessary metallization delay and increase a DRAM performance. The multi-FinFET is one of the candidate to solve this issue and we proposed a simple selective fin formation technique which simultaneously fabricates three different kinds of FETs (FinFET, McFET[3] and planar FET)[4], but it has some problems as follows. (1) Active photo patterning and STI field gap-filling limit the fin-pitch scaling. (2) Commonly used multi gate oxidation process causes consumption of fin width. Initial fin width should be thick enough and it limits fin pitch scalability. (3) It is practically impossible to apply different gate material and threshold voltages of transistors are fixed in a single level. (4) It is difficult to integrate with a conventional SiON gate dielectric planar transistor. In this paper, a spacer transfer through gate polysilicon multi-fin technique is applied to solve problems above. Integration scheme is carefully examined and electric characteristics were evaluated.

2. Integration Design

New features of the proposed technology are, (1) multi-fin structure with TiN gate is fabricated through a gate polysilicon layer for conventional planar transistors, (2) fin width consumption is minimized by consecutive processes of fin formation, cleaning, gate oxidation and TiN gate deposition, (3) fin length is minimized by introducing the DPT (double patterning technique) and it is expected to reduce parasitic source/drain resistance, (4) spacer transfer process[5] is applied to reduce fin-pitch and increase drain current gain.

Fig. 2 shows the schematic process flow of proposed spacer transfer multi-fin formation through the gate polysilicon layer. After gate oxidation and the first gate polysilicon deposition for conventional planar transistors, polysilicon is etched by line/space patterns. Spacers are formed along with polysilicon line patterns. The second polysilicon is depositied to fill spaces. Si substrate under polysilicon is etched to form multi-fin structure. TiN which work-function is at about middle of Si band-gap is deposited to control threshold voltage of CMOS FinFETs. The third gate polysilicon is deposited for planarization and conventional gate formation process is followed. Fig. 3 shows layout and plane view corresponds to Fig. 2. Width and length of the fin are determined by the DPT, which are a spacer along with the 1st photo pattern and the 2nd photo pattern. Fig. 4 shows estimated drain current gain for a proposed technique and a conventional technique normalized by a planar MOS FET. Current gain of a conventional technique is limited by active patterning of photo lithography and minimum space of STI gap-filling. More than 50% current gain is expected for smaller than 50nm design rule with a proposed technique.

3. Result

Fig. 5 shows a vertical SEM image after 2nd polysilicon deposition. 1st polysilicon is patterned in 240nm pitch by ArF dry lithography. 50nm thick spacers are formed along with 1st polysilicon space patterns. Multi-fins are formed by Si substrate etching through 1st and 2nd polysilicon line/space patterns. Si substrate under the spacer is remained as fin structure, so fin width is adjustable by spacer thickness depending on target of the device characteristic. The spacer transfer technique reduces fin-pitch to 120nm, a half of photo lithography pattern pitch as shown in fig. 6. TiN gate electrode is deposited after gate oxidation to control threshold voltage of multi-fin transistors and 3rd polysilicon deposition follows to planarize device topography (fig. 6). Fig. 7 shows plane SEM image of active patterns of sub-word drivers comparing a conventional technique [4]. A number of fins within the same active width increases from 4 to 6 and the fin length is reduced. These improvements are expected to lead to increase of current density due to increase of effective channel width and reduction of parasitic source/drain resistance.

Id-Vg characteristics of the multi-FinFET NMOS with 50nm thick fin and TiN gate is shown in Fig. 8. DIBL is very small as well-fabricated FinFETs. Short channel effect is suppressed down to Lg=70nm as shown in Vth-Lg characteristics of Fig. 9. Vth basically goes down as Wfin gets thinner due to decrease of body charge (Fig. 10), but it shows different characteristics depending on Lg. At large Lg Wfin dependence is relatively small, at Lg=165nm it shows NWE (narrow width effect), and at smaller Lg (90nm), SCE(short channel effect) compensates NWE and shows monotonic Vth dependence on Wfin

4. Summary

A spacer transfer through gate polysilicon multi-fin technique successfully integrated metal gate multi-FinFET and conventional polysilicon gate planar FETs and electrical characteristics of the multi-FinFET are evaluated. 120nm fin-pitch is realized and about 35% drain current gain is expected with 60nm design rule.

Acknowledgement

Authors would like to thank Drs. Donggun Park, Gyoyoung Jin and Won-Seong Lee for discussions, supports and encouragement.

References

[1] T. Ando, ISTF Seminar, 2007.09
[2] Qimonda, "Introducing a New DRAM Technology Roadmap", 2008.02
[3] S. M. Kim, et. al., "Fully Working High Performance Multi-channel Field Effect Transistor (McFET) SRAM Cell on Bulk Si substrate Using TiN Single Metal Gate," *Symp. on VLSI Tech. 2005*, pp.196-197 (11A-2).
[4] M. Yoshida, et. al., "A Full FinFET DRAM Core Integration Technology Using a Simple Selective Fin Formation Technique," Symp. on VLSI Tech. 2006, pp.42-43 (5.2)
[5] Y. G. Choi, et. al., "Sub-20nm CMOS FinFET Technologies,"

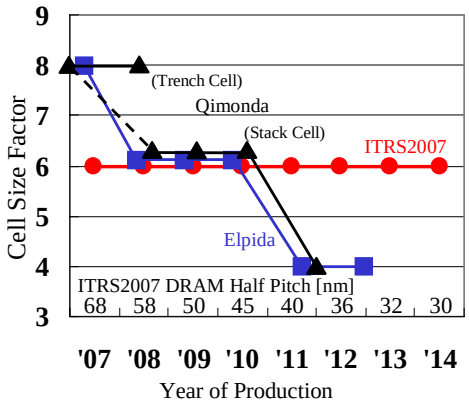

Fig. 1 Trend of DRAM cell scaling. Periphery shrink technology is strongly demanded according to reduction of cell size factor from 8 to 4.

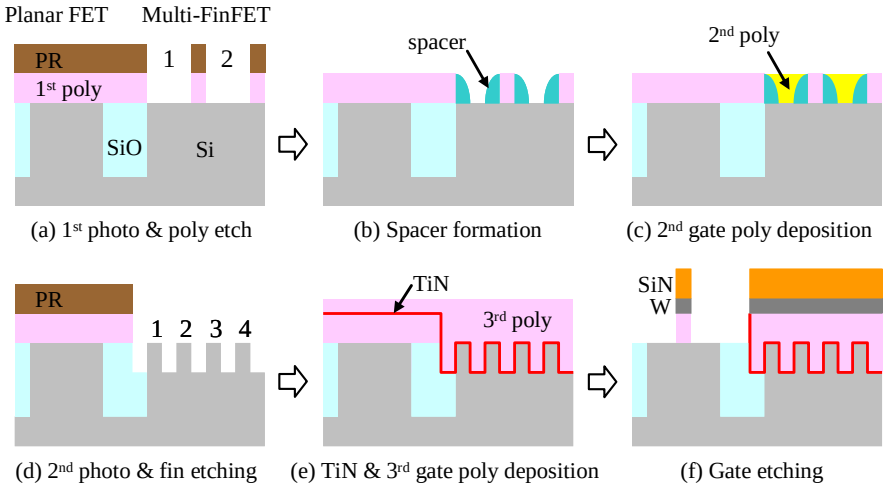

Fig. 2 The process flow of proposed spacer transfer multi-fin formation through the gate polysilicon layer.

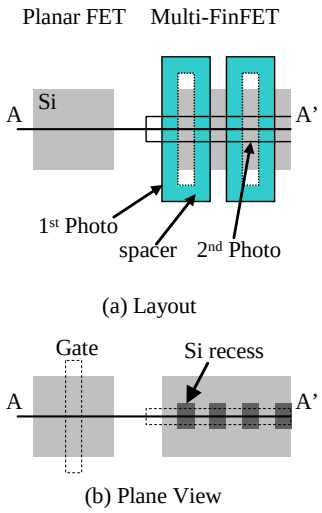

Fig. 3 (a) Layout of proposed scheme. Fin pitch and width are defined by 1st photo and spacer. Fin length is defined by 2nd photo. (b) Plane view after fin etching. A-A' corresponds to the vertical views in Fig. 2.

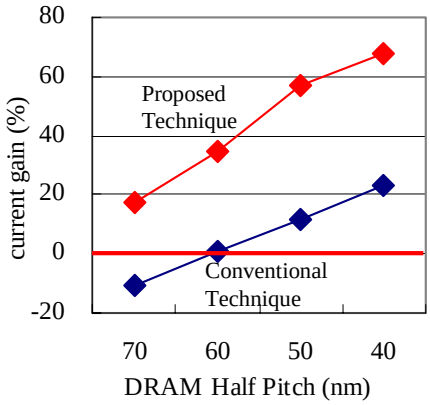

Fig. 4 Estimated drain current gain for a proposed technique and a conventional technique. Limitation of photo lithography, STI gap-filling and fin width consumption by cleaning and gate oxidation make large difference.

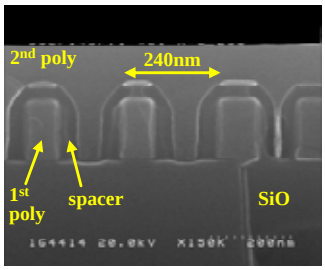

Fig. 5 A vertical SEM image after 2nd poly deposition .

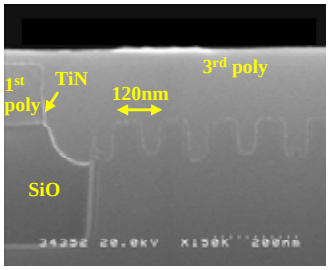

Fig. 6 A vertical SEM image after TiN and 3rd poly deposition.

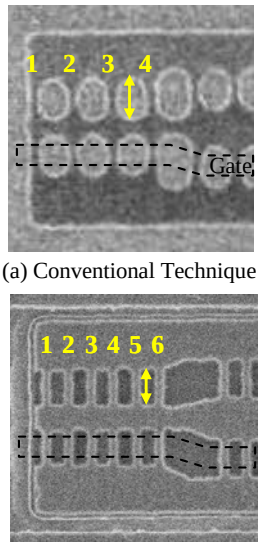

Fig. 7 Plane SEM images of sub-word drivers after fin formation. (a) Conventional technique can make 4 fins, (b) proposed technique can make 6 fins within same channel width and also reduce the fin length.

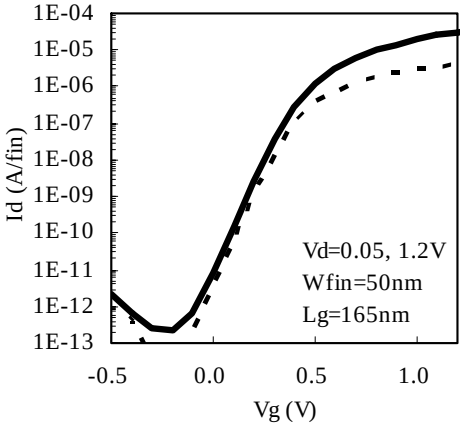

Fig. 8 Id-Vg characteristics of multi-FinFET NMOS with TiN gate at 85C.

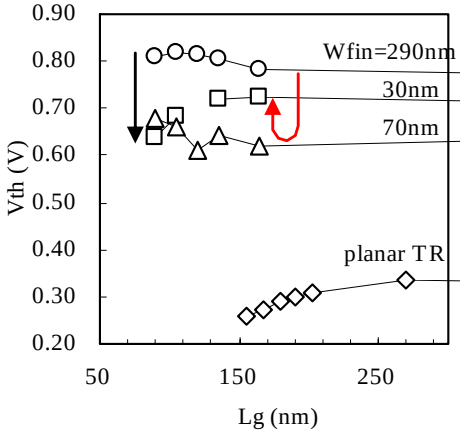

Fig. 9 Vth-Lg characteristics of multi-FinFET NMOS with various Wfin.

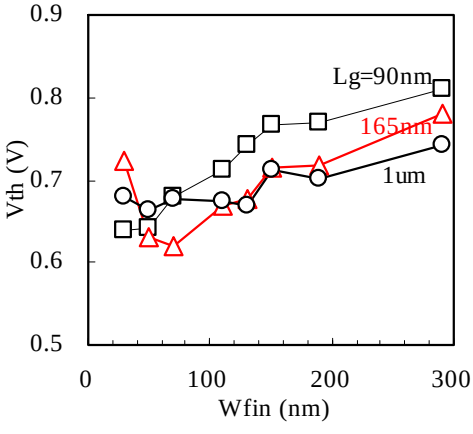

Fig. 10 Vth-Wfin characteristics of multi-FinFET NMOS with various Lg.