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Improving Read Disturb Characteristics by Self-boosting Read Scheme for MLC NAND Flash Memories

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1. Introduction

In order to meet the ever-increasing market demand for high density flash memory, the continued scaling of NAND flash devices will remain essential in the future. However, the scaling of flash memory cells causes reliability issues, among which are cycling induced damaging of the tunnel oxide, which causes data retention problems, read disturb, and so on. So far, endurance and HTS characteristics have been regarded as the most important reliability issues of flash memory. In the case of SSD (Solid-State Drive) using NAND, the repeated read access of a specific block frequently occurs. Therefore, the degradation of read disturb characteristics is expected to become another important reliability issue for future NAND flash memories. There are two key process parameters which determine the read disturb characteristics. One is the tunnel oxide thickness. From measurement results of 60nm NAND device, as shown in Fig. 1 (a), better read disturb characteristics are achieved for thicker tunnel oxides since in this case the leakage current of tunnel oxide is suppressed due to decreased electric field across tunnel oxide. However, both HTS and P/E cycling degradation limit the scaling of tunnel oxide thickness because of the increased oxide charge and interface trap [1], as shown in Fig. 1 (b) and (c). The other parameter is the field height (F/H) which affects the distance between the active region and the control gate (Fig. 2 (a)). By increasing the field height, the read disturb can be suppressed as the effect of the reduced electric field between the active region and control gate (Fig. 2 (b)). However, the increased F/H results in the reduction of coupling ratio caused by both decreased capacitance between control and floating gates and increased cell to cell interference [2], as shown in Fig. 2 (c). Consequently, it has come to be difficult to sustain the reliability of scaled NAND devices only by controlling the device structure and process parameters. To overcome these reliability issues and to further scale NAND devices, a new operation scheme and circuit design as well as device and process innovations are required. In this paper, we propose a new NAND string and its read operation scheme using self-boosting to improve the read disturb characteristics. The proposed scheme was successfully demonstrated using 60nm NAND technology.

2. Conventional Read Scheme

Fig. 3 shows a conventional NAND cell operating conditions for reading. During read operation, a cell is typically read by applying a voltage to the word line to which the control gate of the cell is connected, applying a pre-charging voltage to the bit line to which the drain of the cell is connected, grounding the source, and sensing the bit line current. The unselected strings are discharged to ground for noise shielding. In general, the read disturb is worst at unselected BL because the electric field across tunnel oxide becomes maximum. Fig. 4 shows simulation results of electric fields as a function of read voltage and F/H. As the read voltage is increased and F/H is decreased, read disturb characteristic get worse due to the increased the electric field.

3. Proposed NAND Flash and Self-boosting Read Scheme

Fig. 5 shows a concept of the proposed NAND to improve read disturb. Two additional switches with different Vth for each using dummy cells are placed. Unlike read operation of conventional NAND, V_{CC} is applied on the unselected BL instead of 0 V and V_{CC} is applied on the SSL transistors instead of Vread. The selected BL is turned on and the unselected BL is turned off [3]. Thus, channel voltages of unselected BLs are boosted when Vread voltage is applied to the control gates. This boosted channel voltage prevents F-N tunneling in unselected BL. It leads to significantly improve read disturb compared to conventional scheme. The overhead of additional dummy cells can be minimized as scaling NAND device [4].

4. Implementation and Performance

Fig. 6 shows the structure of proposed NAND device with dummy cells and its new read timing diagram and bias conditions. To implement two switches with each different Vth, two dummy cells which are identical to normal memory cell are additionally placed between GSL transistor and edge memory cell WL [0]. The V_{TH} of dummy cells is set to be -2V and 2V, respectively. Before applying V_{CC} to SSL and Vread to unselected WL, the BL voltages 0.7V, V_{CC} are applied in advance at t1. When Vcc, Vr, Vread and 1V are applied to SSL, selected WL, DWL2 and DWL1 at t2, channel voltage of unselected BL is precharged to V_{CC}-V_{TH} and then becomes a floating node. When Vread is applied to unselected WLs and GSL, the channel potential of unselected BL is raised due to the capacitive coupling. Thus, the read disturb is suppressed through a self boosted read scheme. Table 1 summarizes the proposed read conditions compared to the conventional conditions. Fig. 7 shows a simulated electrical field of conventional and the proposed NAND during read operation. The electrical field of the proposed NAND is significantly decreased by about 3MV/cm as a result of the boosted channel potential. Also, Fig. 8 (a), (b) show simulation results of the floating gate charge and V_{TH} shift as a function of the numbers of read cycles for differing field heights. Even though the field height is decreased, the proposed NAND flash is insensitive to read cycling due to the decreased electric field. The results can increase a degree of freedom for designing future scaled NAND device. Fig. 9 shows measured V_{TH} shift of disturbed memory cell as a function of read cycling and read voltages. In case of high Vread = 8.5V, read cycles = 25M, the V_{TH} shifts of the proposed NAND is more than 2V lower compared to conventional NAND. Also, the proposed NAND is more immune to P/E cycling at Vread = 7V, as shown in Fig. 10. Thus, the results described above proves excellent read disturb characteristics of the proposed NAND.

5. Conclusion

We proposed a new NAND device and its read operation using self boosting as a solution for scaled NAND flash memories. The proposed read scheme which includes the combination of optimized bias voltage and adjusted VTH of dummy cell contributes to improve dramatically the read disturb of memory cell. The proposed NAND was successfully demonstrated by simulation and experiment in fabricated 60nm NAND device.

Reference

[1] K-N. Kim, et al, IEDM, pp. 27-30, 2007 [2] Y-S Shin, et al, VLSI, pp. 156-159, 2005 [3] K-D Suh, et al., JSSC, Vol. 31, No. 11, pp.1149-1156, 1995 [4] K-T Park, et al., SSDM, pp. 298-299, 2006

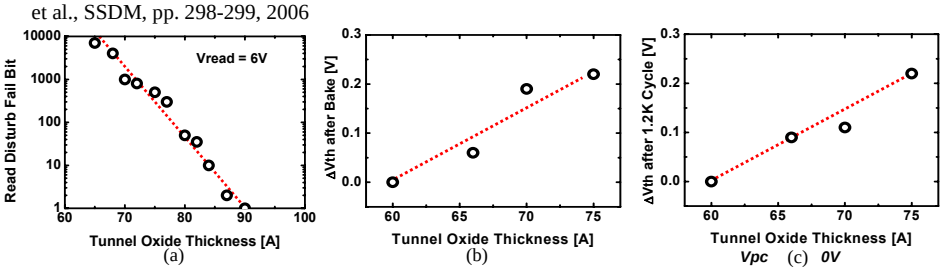


Fig. 1 Measured (a) Read disturb (b) HTS (c) Endurance as a function of tunnel oxide thickness at 60nm NAND

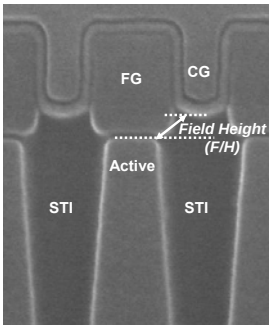


Fig. 2 (a) Cross-sectional view of a 60nm NAND Device

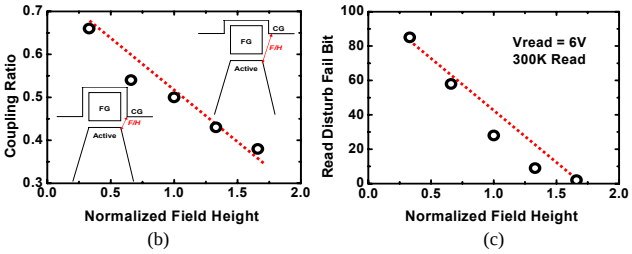


Fig. 2 Measured (b) Coupling ratio (c) Read disturb fail bit as a function of field height at 60nm NAND

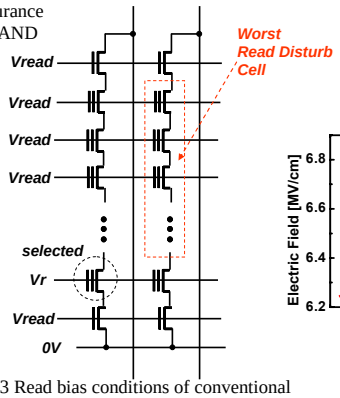


Fig. 3 Read bias conditions of conventional NAND device

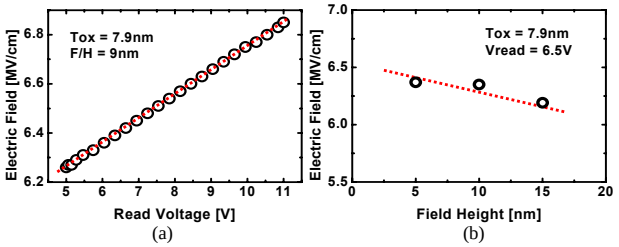


Fig. 4 Simulated Electric field as a function of Read Voltage and F/H (Field Height)

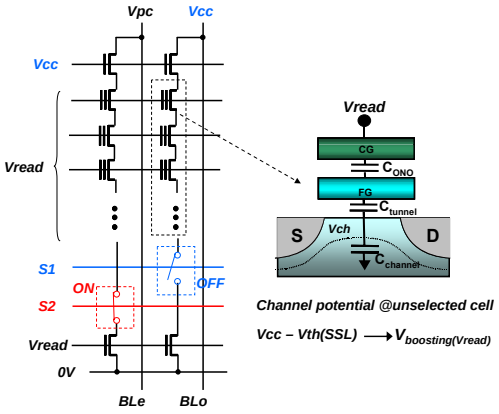
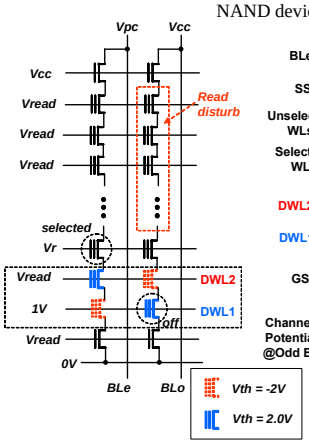


Fig. 5 Concept of proposed NAND read using self-boosting



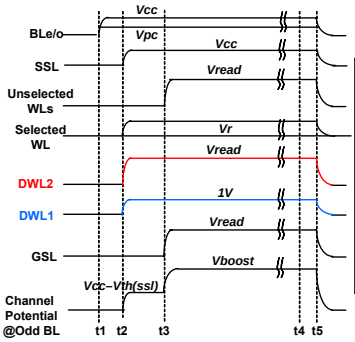


Fig. 6 Read bias and timing conditions for proposed NAND

	Conventional Read Condition	Proposed Read Condition
BL	0V	Vcc
SSL	Vread	Vcc
Unselected WL	Vread	Vread
Selected WL	Vr	Vr
DWL2	Vread	Vread
DWL1	Vread	1V
CSL	0V	0V

Table 1. Conventional and proposed read conditions (Vr : read voltage for selected WL, Vread : read voltage for unselected WL)

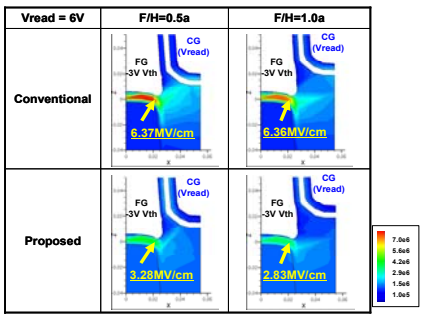


Fig. 7 Simulated read electrical field of conventional and proposed NAND according to the field height at Vread=6V.

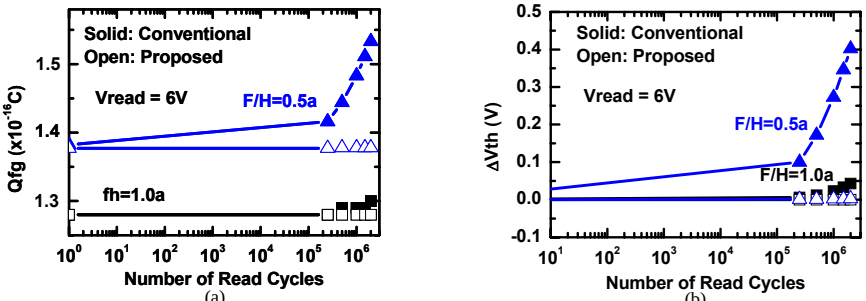


Fig. 8 Simulated (a) the number of floating gate charge, (b)Vth shift as a function of the number of read cycles

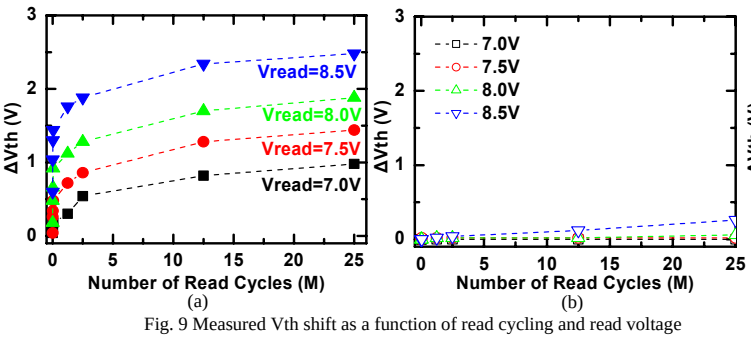


Fig. 9 Measured Vth shift as a function of read cycling and read voltage (a) Conventional NAND (b) Proposed NAND

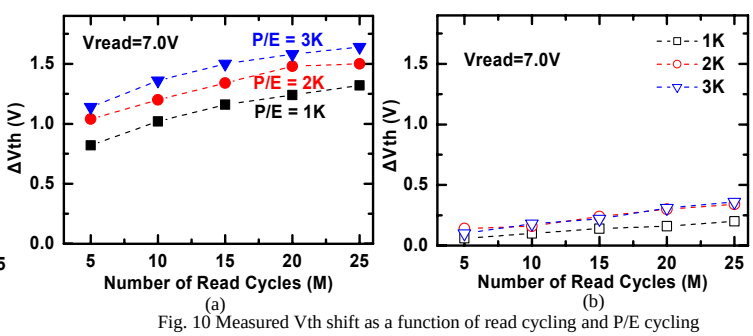


Fig. 10 Measured Vth shift as a function of read cycling and P/E cycling (a) Conventional NAND (b) Proposed NAND