Memory Characterization of MOS Memory Device with High Density Self-Assembled Tungsten Nanodots Floating Gate and HfO₂ Blocking Dielectric

Yanli Pei¹, Masahiko Nishijima², Takafumi Fukushima³, Tetsu Tanaka³ and Mitsumasa Koyanagi³

¹International Advanced Research and Education Organization, Tohoku University

6-6-03 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8578, Japan

Phone: +81-22-795-4031, E-mail: sdlab@sd.mech.tohoku.ac.jp

² Institute for Materials Research, Tohoku University

³Dept. of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University

1. Introduction

Metal nanodots floating gate flash memory have attracted much attention for the future nonvolatile memory (NVM) device. Compared with conventional semiconductor nanocrystal floating gate, the metal nanodots floating gate show lots of advantages such as higher density of energy state and wide range of available work functions [1]. However, they will face some challenges such as prevention of metal/oxide reaction and metal diffusion into tunneling and blocking dielectrics during fabrication process, which may potentially degrade the device performance, and fabrication of high density nanodots to overcome the fluctuation of electrical characteristics among devices [2].

To improve the electrical performance of flash memory devices, efforts are also made to replace the SiO_2 blocking oxide with high dielectric constant materials. This improves controllability of gate to write/erase data, resulting in lower programming voltages [3].

In this work, to solve above issues, the metal–oxidesemiconductor (MOS) memory capacitor with a floating gate of high density self-assembled tungsten nanodots (W-NDs) dispersed in silicon nitride and HfO_2 blocking dielectric was fabricated. The physical and electrical properties were discussed in detail.

2. Experiment

The MOS memory capacitor with W-NDs was fabricated as the following process. P-type Si (100) substrate with a resistivity of 5~10 Ωcm was used. An 8-nm-thick W-NDs layer was deposited on 5-nm-thick tunneling SiO₂ by self-assembled nanodot deposition (SAND) method [4]. In this method, tungsten chips placed on a Si₃N₄ target were cosputtered in high-vacuum RF sputtering equipment. The W-NDs film was annealed at 800°C in high vacuum ambient. The blocking oxide layer is 30-nm-thick HfO₂ formed by RF sputtering equipment, followed by 600°C annealing. Finally, Al electrode with a diameter of 0.3 mm was evaporated, followed by post-metallization annealing at 400°C. In this study, the MOS capacitor without W-NDs layer was also fabricated simultaneously. Figure 1 shows the schematic cross section of a W-ND memory capacitor. The physical characteristics of W-NDs were evaluated by high-resolution transmission electron microscopy (HRTEM) and x-ray photoelectron spectra (XPS). The memory properties were investigated using an Agilent B1500A semiconductor parameter analyzer at room temperature.



Fig. 1 Schematic cross section of W-ND MOS memory capacitor.

3. Results and Discussion

A cross-sectional HRTEM image of HfO₂ /W-NDs /SiO₂/ p-Si stacked structure is shown in Fig. 2 (a). The excellent interface at SiO₂/W-NDs is observed, indicating that the W-ND is not diffused into the tunneling oxide even after 800°C anneal. The thickness of HfO₂ is about ~30nm with partially crystalline. To further confirm the W-ND structure, a cross-sectional HRTEM image of W-NDs/SiO₂/p-Si with 800°C anneal was shown in Fig. 2 (b). The spherical and separated W-ND with a size of 1.0~2.0nm are clearly observed embedded in the silicon nitride layer. The distributed area density of W-ND is ~10¹³ cm⁻² estimated by HRTEM analysis. Crystallized W-ND with lattice fringes was obviously visible in the inset of Fig. 2 (b).

To confirm the chemical composition of W-NDs after 800°C anneal, the XPS spectrum of W4f in shown in Fig. 3. In a previous study, a tungsten film showed a spin-orbit doublet due to W $4f^{7/2}$ at 31.4 eV and W $4f^{5/2}$ at 33.6 eV, which represent W⁰ [5]. With processing of metal/oxide reaction, W4f peaks were shifted to high binding energy. From Fig. 3,



Fig. 2. HRTEM images of (a) HfO_2/W -NDs /SiO₂/Si stacked structure and (b) W-NDs/SiO₂/Si stacked structure.



Fig. 3. W4f level XPS spectrum of 8-nm-thick W-NDs in silicon nitride.



Fig. 4. C-V curves of W-ND MOS memory capacitor measured at different frequencies.

we found that the W-NDs have high metallic states and partly oxidized composition, which is identical to the high binding energy. Compared with W-ND embedded in silicon oxide reported in ref. [4], the oxidation of tungsten was suppressed by silicon nitride markedly.

In Fig. 4, we show the capacitance-voltage (C-V) characteristics of W-ND MOS memory capacitor, measured at different frequencies with a range of 1KHz ~1MHz. The frequency independence of C-V curves suggested that the memory window is not due to the interface traps. Figure 5 shows the C-V measurement with bi-directional voltage sweeping from 8 to -8V and from -8 to 8V for MOS memory capacitors with and without W-NDs layer. Considering the small C-V hysterisis of MOS capacitor without W-NDs layer, the larger counterclockwise hysterisis for W-ND MOS memory capacitor is attributed to the charge exchanging between W-ND and silicon substrate. From the analysis of C-V curve for capacitor without W-NDs layer, the dielectric constant of HfO₂ was estimated about $\sim 18\epsilon_0$ and equivalent oxide thickness (EOT) about ~7nm. We summarized the flat band voltage as a function of sweeping gate bias voltage for W-ND MOS memory capacitor in Fig. 6. It is found that programming and erasing are from Vg=±5V. At Vg=±9V, the memory window of ~5.5V was obtained. We have calculated the electron density charged in W-NDs by formula as reference [6]. At memory window of ~5.5V, the extremely high trapped electron density was obtained about $\sim 2.7 \times 10^{13}$ /cm². The result indicated that one W-ND can store 2 or more electrons. The lower programming voltage and larger memory window



Fig. 5. High-frequency (1MHz) C-V curves for MOS memory capacitors with and without W-NDs layer.



Fig. 6. Flat band voltage as a function of sweep gate bias for W-ND MOS memory capacitor.

indicated that the HfO₂ blocking dielectric with high dielectric constant leads to the coupling to the tunneling oxide effectively.

4. Conclusions

Crystallized W-NDs dispersed in silicon nitride were prepared by SAND with extremely high density $(1x10^{13}/cm^2)$ and small size (1.0~2.0nm), successfully. XPS results show that the high metallic states of tungsten were remained after 800 °C anneal due to the surround silicon nitride. MOS memory capacitor with W-ND floating gate and HfO₂ blocking dielectric was fabricated. A large hysteresis memory window of ~5.5V at a low sweeping gate voltage of \pm 9V was obtained, response to the high trapped electron density of ~2.7x10¹³/cm². The results suggested that memory with floating gate of W-ND in silicon nitride and high-k blocking dielectric become a good candidate for future NVM application.

Acknowledgements

This work was partly supported by a Grant-in-Aid. for Scientific Research on Priority Area (No. 18063002) from the Ministry of Education, Culture, Sports, Science, and Technology in Japan.

References

- [1] J. H. Kim et al., Appl. Phys. Lett. 92 (2008) 013512.
- [2] B. De Salvo et al., IEDM (2003) 999.
- [3] J. Chen et al., IEEE Trans. Electr. Dev. 51 (2004) 1840.
- [4] Y. Pei et al., Jpn. J. Appl. Phys. 47 (2008) 2680.
- [5] T. H. Fleisch et al., J. Chem. Phys. 76 (1982) 780.
- [6] H. Hanafi et al., IEEE Trans. Electr. Dev. 43 (1996) 1553.