Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 244-245

J-2-6

Temperature Effects on Recrystallization and Improvements of Pure Gadolinium (Gd) Nanocrystal (NC) for Flash Memory

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1. Introduction

In recent years, floating gate (FG) memory devices [1] were used in all kinds of electronic production for non-volatile data storage application. Unfortunately, for conventional FG memory, device scaling limitation and poor data retention time are two major issues needed to be overcome. The nanocrystal (NC) memory devices [2-3] which with discrete charge storage nodes for the resolution of device scaling and to improve the retention time have been proposed to be a possible candidate for the replacement of the FG memory. However, for NC memories, the most challenging tasks are how to maintain acceptable charge capability of the discrete storage nodes and fabricate NC with constant size, high density, and uniform distributions.

In this study, we propose a pure Gadolinium (Gd) NC memory which is optimized to exhibit high Gd-NC density ($8.5x10^{11}/cm^2$), large P/E window (>4V) and good data retention [4] (>85°C) for the first time. The Gd-nanocrystal memory is fully compatible with the current CMOS technologies and can also be applied into future high density charge storage application.

2. Experiment

The memory cells were fabricated on n-type silicon (100) wafers. First, a 3 nm tunnel oxide was thermally grown in a horizontal furnace system after standard RCA clean process. Then, a 10 nm amorphous Gd_2O_3 wetting layer was deposited by sputtering with pure Gadolinium (99.9% pure) target in oxygen (O_2) and argon (Ar) mixture ambience. After the deposition of Gd_2O_3 wetting layer, these thin films were then treated in N_2 ambient at 800 to 950°C for 30s, respectively. A SiO_2 blocking oxide with a thickness of about 9nm were deposited by plasma enhance chemical vapor deposition (PECVD). Subsequently, Al deposition, gate patterning, and backside Al deposition were completed to fabricate the Gd-NC memory capacitor (Fig. 1). Finally, we have used the transmission electron microscopy (TEM) to analysis the material properties and HP4285 LCR meter to characterize the P/E performance by measuring the high-frequency capacitance-voltage (C-V) curves.

3. Results and Discussion

Fig. 2(a) and (b) show the cross section TEM images of Gd-NCs embedded in a Gd_2O_3 layer with post deposition annealing (PDA) at 900 and 850°C respectively. The mean size of Gd-NCs was measured to be about 15 and 9nm respectively. There exists a Gd_2O_3 layer between Gd-NC and tunneling oxide for the 850°C annealed sample, which is not observed for the 900°C annealed one. In addition, the lattice constant of the Gd-NC was calculated to be about 0.3nm (Fig. 2(c)), which is identical to the pure Gd atom (a=0.36nm). The NCs were also identified to be Gd phase by analysis of electron diffraction pattern as shown in Fig. 2(d). Fig. 3 shows the PDA temperature dependence on Gd-NC density obtained from top view TEM image in inset. It is observed that the Gd-NC density is optimized to be $8.5\times10^{11}cm^{-2}$ at 850°C and the mean size is uniform for 9nm. The C-V hysteresis curves of Gd-NC memories with different PDA temperature are presented from -11V to +11V (Fig. 4) and showed that the device exhibits the best storage capability for PDA at 850°C, which is proved by the highest Gd-NCs density as revealed in Fig. 3.

Fig. 5 demonstrates the data retention characteristics of Gd-NC memories with different PDA temperature at room temperature measurement. The charge loss is defined as the percentage of cell window narrowing. To study the blocking oxide characteristics, the positive bias was applied to the gate for constant electric field stress as shown in Fig. 6 (flat-band) and 7 (E=2.8MV/cm). For all the samples, PDA treated at 950°C sample presents the large charge loss especially at E=2.8MV/cm. The high PDA temperature will enlarge the NC size leading to high probability of electron tunneling from NC to gate by blocking oxide defect. Fig. 8 and 9 display the charge loss characteristics of the samples measured at 55 and 85°C respectively. Less charge loss of 850°C annealed sample is observed because of the existence of Gd_2O_3 layer between Gd-NCs and tunneling oxide (Fig. 2 (b)). In Fig. 10, activation energy of Gd-NC memories was extracted and found the sample with 850°C PDA treatment is less sensitive to thermal activation that exhibits superior data retention properties. Schematic band diagrams of Gd charge storage dots under constant electric field and thermal activation modes for 850 and 900°C PDA treatment are shown in Fig. 11.

4. Conclusions

In this paper, we investigated the pure Gd-nanocrystal memories with optimized PDA treatment temperature for the first time. The Gd-NC memories with 850°C PDA treatment showed large memory window and excellent retention characteristics. This memory can be used for next generation flash application.

References

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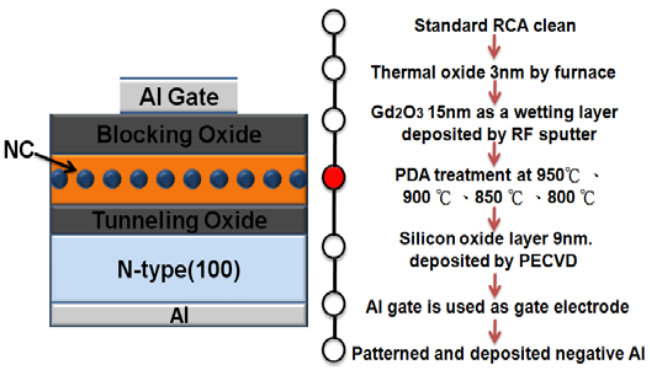

Fig. 1 Schematic cross section and process flow of Gd-nanocrystal memory structure.

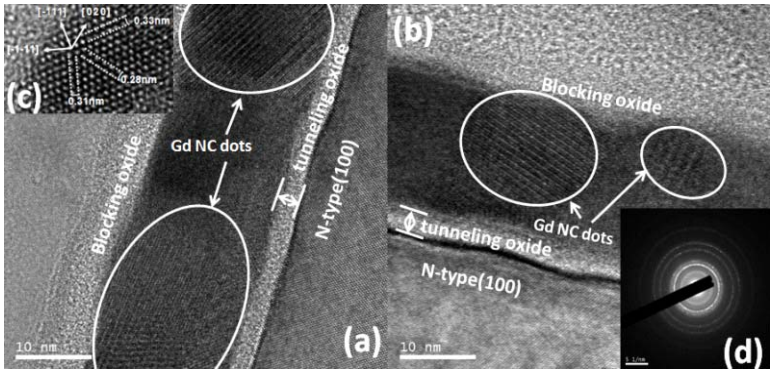

Fig. 2 The HRTEM images of Gd-NC memory with PDA treatment at (a) 900℃ and (b) 850℃ respectively. The lattice constant (c) and electron diffraction pattern (d) of Gd-nanocrystal were in inset figure.

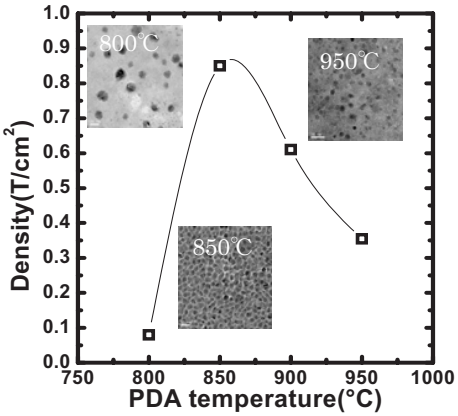

Fig. 3 Gd-NC density dependence on PDA temperature. The density was obtained by the top view TEM images.

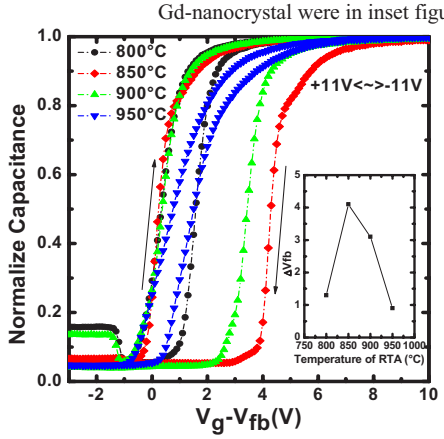

Fig. 4 C-V hysteresis of Gd-NC memories with 800 to 950℃ PDA treatment swept from -11V to +11V. Memory window of all samples was shown in inset.

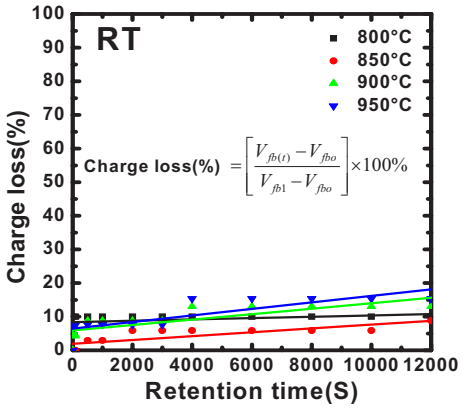

Fig. 5 Retention characteristics of Gd-NC memories measured at room temperature. The charge loss was defined as the percentage of cell window narrowing.

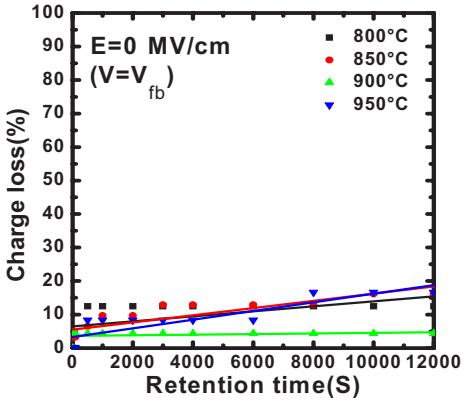

Fig. 6 Retention characteristics of Gd-NC memories with constant electric field stress (flat-band).

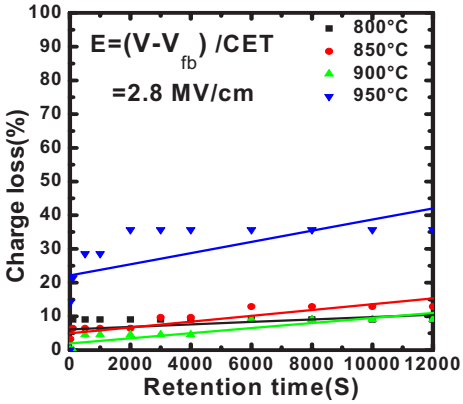

Fig. 7 Retention characteristics of Gd-NC memories with constant electric field stress (E=2.8MV/cm).

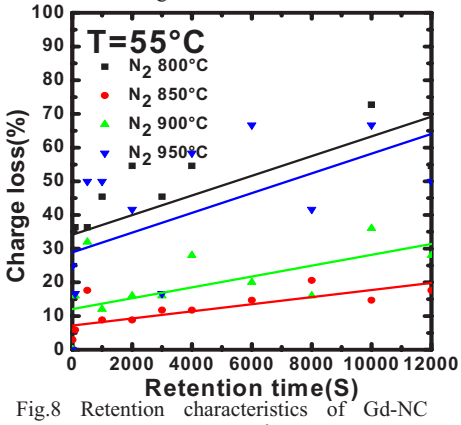

Fig.8 Retention characteristics of Gd-NC memories measured at 55℃. High thermal activation will contribute to large charge loss.

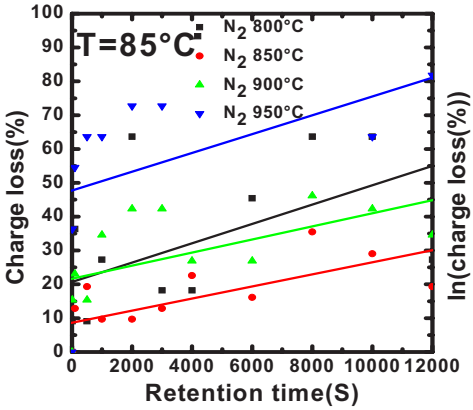

Fig. 9 Retention characteristics of Gd-NC memories measured at 85℃.

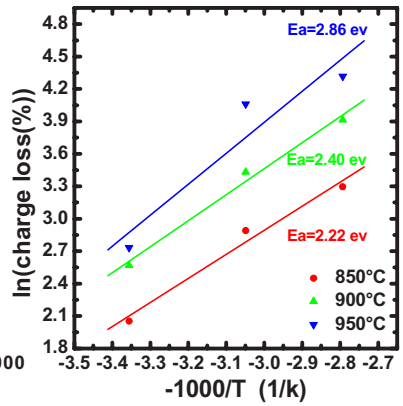

Fig. 10 Arrhenius plot of charge loss for GC-NC memories. The plots were obtained from charge loss characteristics at retention time for 10ks.

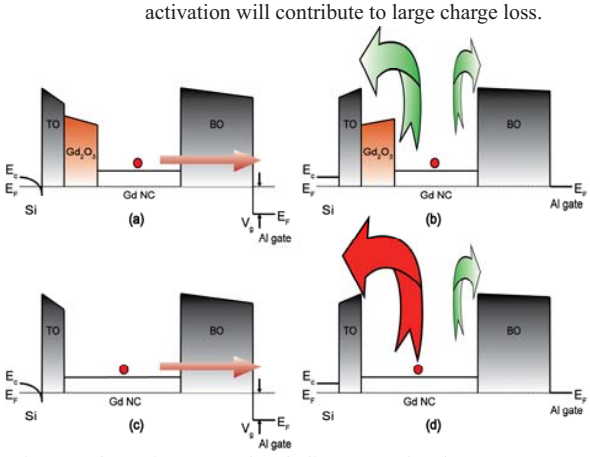

Fig.11 Schematic energy band diagrams of Gd-NC memory structure with (a)&(b) 850, and (c)&(d) 900℃ PDA treatment. The indicated retention states were kept at (a)&(c) constant electric field, and (b)&(d) high thermal activation environment.