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Three Dimensional Flash Memory with Bit Cost Scalable Technology for the Future Ultra High Density Storage Devices

Hideaki Aochi, Masaru Kito, Yoshiaki Fukuzumi, Masaru Kido, Hiroyasu Tanaka, Yasuyuki Matsuoka, Yosuke Komori, Megumi Ishiduki, Yuzo Nagata*, Ryota Katsumata, Yoshihisa Iwata, and Akihiro Nitayama

Center for Semiconductor Research & Development, TOSHIBA Corporation, Semiconductor Company

*Toshiba Information Systems (Japan) Corporation

8 Shinsugita-Cho Isogo-Ku Yokohama, 235-8522, Japan

Phone +81-45-776-5606, E-mail: hideaki.aochi@toshiba.co.jp

1. Introduction

Three dimensional memories are gathering increasing attention as future ultra-high density memory technologies to keep a trend of increasing bit density and reducing bit cost. Several candidates of the technologies for the future three dimensional non-volatile memory were proposed, as shown in figure 1, such as cross point cell with resistive change memory and diode [1], simply stacked two dimensional array structures [2,3], Bit-Cost Scalable (BiCS) flash technology [4,5] and VRAT with PIPE [6]. Disadvantage of the cross point cell and simply stacked two dimensional arrays is that the process cost to build one layer of memory array is relatively high because each layer needs several lithography steps and the other processes. This is the reason why the efficiency of cost reduction by stacking layers of memory array is not so good. On the other hand, the last two technologies listed above realize a multi-stacked memory array with a few constant number of critical lithography steps regardless of the number of stacked layers, and make continuous bit cost reduction possible.

In this paper, the concept and the other technology items of BiCS flash are reviewed.

2. Concept of BiCS flash

Figure 2 shows the concept of BiCS flash memory. Whole stack of electrode plates are punched through and plugged with SONOS-type memory films and poly-silicon at one time to form a series of vertical FETs which act as a NAND string of SONOS-type memories [4]. Several rows of NAND string share control gates and the lower select gate. Upper select gate is formed as line and space to take a role of row select line. Due to the punch and plug process, sequence of FET formation is completely opposite to the conventional FET, i.e., gate dielectric films are deposited on the side wall of gate hole followed by deposition of channel Si as shown in figure 3. The bottom of memory string is connected to the common source diffusion formed on the silicon substrate. Figure 4 shows the birds-eye view and cross section SEMs of fabricated test chip of BiCS flash with 4 layers of control gates.

3. Macaroni FET and SONOS-type memory films

As we reported, one of the most serious concern is that channel of vertical FET is poly Si. To improve the FET characteristics, "Macaroni" type FET is proposed [5]. Figure 5 shows the schematic of "Macaroni" FET. By reducing the thickness of channel poly-Si less than the width of depletion region induced by gate bias, distribution of V_{th} is dramatically improved as shown in Figure 6.

Figure 7 shows that sub-threshold slope becomes steeper and on-current increases by thinning Si thickness of "Macaroni FET".

We reported SiN-base gate dielectric film is better to get good compatibility with BiCS process integration [5]. The other important point for SONOS-type memory films is that the top down view of string is a circle as shown in figure 8. In this case, radius of curvature of tunnel oxide is less than that of block oxide, as is well known, that means the electric field on tunnel oxide is much larger than that of block oxide. As the result, BiCS does not need high-k material as block oxide even for the case that both of program and erase operation is done by FN current as shown in figure 8. Retention result for oxide block film is also excellent as shown in figure 9

4. Operation and disturb for BiCS flash

A single memory cell is accessed at the intersection of a control gate and a NAND string, which is selected by a bit line and an upper select gate. Erase operation is done with holes generated by GIDL at the junction edge of upper and lower select gates as shown in Figure 10. Figure 11 shows that higher concentration of junction generates more GIDL, holes and ΔV_{th} . The result of program and erase for each single cell on a string in fabricated test chip is shown in figure 12.

In case of BiCS flash, there are many unselected strings which are stressed by V_{prog} , V_{pass} or V_{read} in the same time with selected string because some rows of strings are sharing control gate. However high enough voltage boost happens due to no coupling between pillar and substrate when both of upper and lower select gates isolates pillar from bit line and source line well, so that disturbs on the unselected string are not serious concern.

5. Conclusions

BiCS flash is one of the most cost effective memories in the currently proposed three dimensional non-volatile memories. It does not require new material for memory cell and there is no serious concern for disturbs. It is one of the strong candidates for the future ultra high density storage devices.

References

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- [6] J.Kim et.al. VLSI Symp. Tech Dig., pp122-123, 2007.

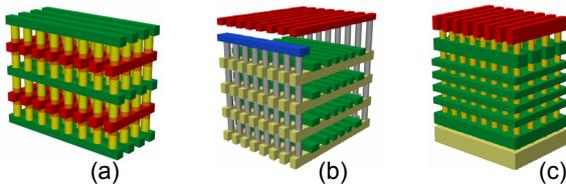


Fig.1 Examples of 3-D memory array. (a) Cross point cell (b) Simply stacked planar cell and (c) BiCS flash

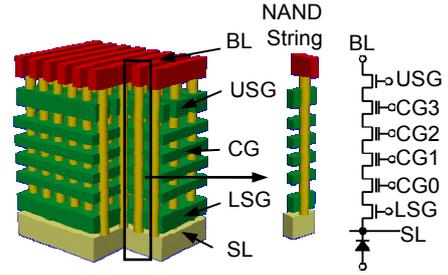


Fig.2 Concept of BiCS Flash.

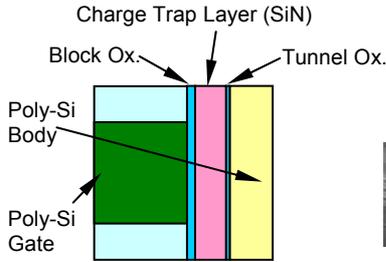


Fig.3 "Gate first" process for FET fabrication. Gate dielectric films are deposited on the Gate followed by channel Poly Si deposition.

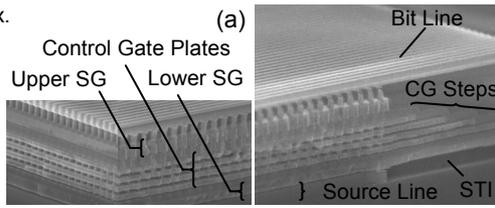


Fig.4 Birds-eye view(a) and cross section (b) SEM picture of fabricated BiCS flash in test chip.

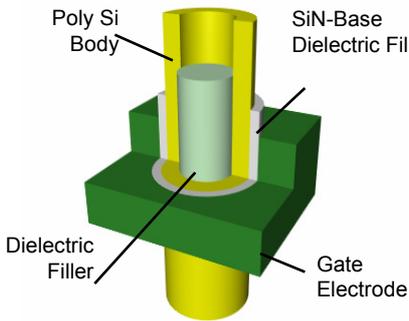
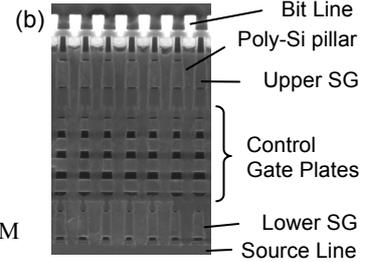


Fig.5 Schematic illustration of "Macaroni" vertical FET.

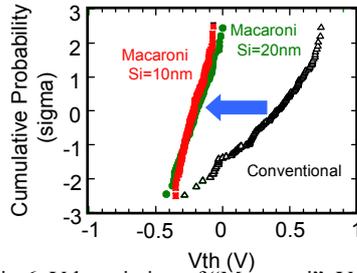


Fig.6 V_{th} variation of "Macaroni" Vertical FET. Thinner Si shows better results.

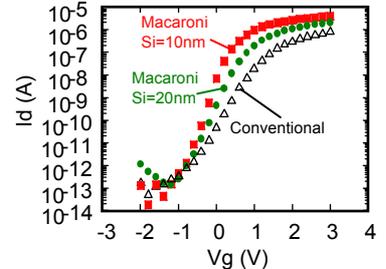


Fig.7 I_d - V_g characteristics of "Macaroni" vertical FET. Thinner Si shows better results.

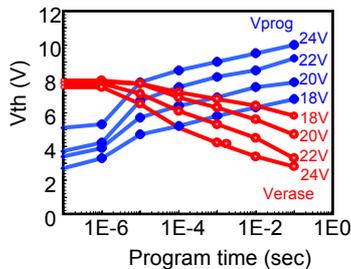


Fig.8 Program/Erase characteristics of BiCS with oxide block film. Radius of curvature difference between tunnel ox. and block ox. enables erase operation by FN current.

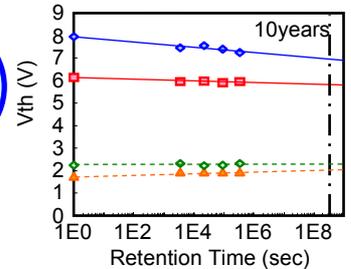


Fig.9 Data retention characteristics of BiCS with oxide block film.

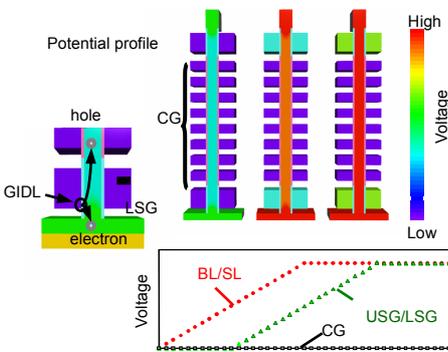


Fig.10 Schematic illustration of erase operation of BiCS Flash. Hole generated by GIDL at the SG edge raises the potential of pillar up.

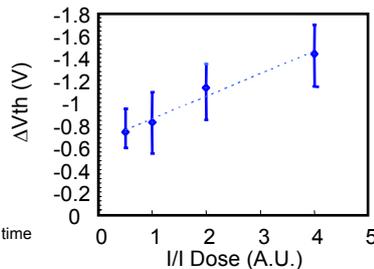


Fig.11 V_{th} shift by erase bias as a function of source/drain I/I dose. Higher concentration of junction generates more GIDL, holes and larger V_{th} shift.

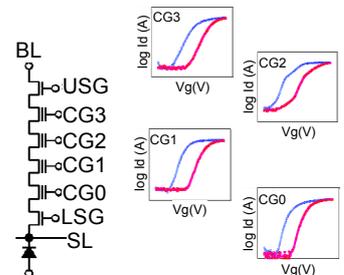


Fig.12 Result of program and erase for each single cell on a string in the fabricated test chip.