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Low Temperature GAA Poly-Si Nanowire TFT SONOS Memory for MLC Application

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1. INTRODUCTION

Polycrystalline silicon (poly-Si) TFT has been widely employed in the active matrix LCD displays. Nowadays, in order to integrate the functionality of memory into an entire system on top of the panel (SOP), great efforts have been made in researching TFT memories, such as TFT SONOS nonvolatile memories [1, 2]. However, the performance of the TFT is not yet comparable to single crystalline cells. The TFT devices usually have the issues of poor subthreshold property and slow memory speed, which are because of the rough grainy channel surface and many dangling bonds along the grain boundaries. Yamauchi *et al.* has shown great improvement of TFT device performance by increasing the grain size in the channel [3]. The reason could be related to the negative effect induced by poly-Si grain is shrinking by reducing the absolute number of grains and grain boundaries in the channel. Hence, in this point, the narrow channel of fin or nanowire is worthy of being introduced into the TFT memory to bring down the negative effect of the grain. As reported by Im *at al.*, such narrow channels is possible to contain only one poly-Si grain when the cross-sectional channel dimension scales to only tens of nanometers [4].

In this work, we demonstrate gate-all-around (GAA) polycrystalline silicon nanowire thin film transistors (TFT) SONOS nonvolatile memory device using low temperature CMOS compatible processes. The fabricated GAA poly-Si nanowire SONOS exhibits excellent subthreshold behavior and fast memory speed, as fast as 1μs. Both the static and transient device characteristics are found dependent on the nanowire width, and the device with smaller width shows better performance. The ability to achieve large memory window enables the GAA TFT memory device suitable for the multi-level cell (MLC) application.

2. FABRICATION

The process flow of nanowire TFT SONOS device is given in Fig. 1. Shown in Fig. 2 are the schematic diagrams of main process steps. We fabricated the poly-Si nanowire similarly with our previous work on single crystalline Si nanowire devices [6], but with all process temperature reduced to adapt the low temperature TFT application. Amorphous silicon (α-Si) film with thickness of 600Å was first deposited on 4000Å SiO_2. Fin structure was then patterned and etched as active region. Steam oxidation at 730ºC for 30 minutes, which was the largest thermal budget in this work, was performed to oxidize the fin partially. It left a single nanowire which was wrapped in the oxide. The nanowire was released in DHF, as the SEM image shown in Fig.3, and followed by the deposition of tunnel oxide, nitride and blocking oxide (ONO: 5nm/15nm/11nm) using PECVD at 400ºC. After gate electrode definition, S/D implantation and activation (580ºC for 24 hours), contact metallization and forming gas sintering were subsequently performed to conclude the fabrication process. The α-Si nanowire was crystallized into poly-Si nanowire by solid phase crystallization during this long duration dopant activation step.

3. RESULTS AND DISCUSSION

Fig. 4 shows a cross-sectional TEM image of GAA nanowire TFT SONOS device, with a minimum poly-Si nanowire width of 23nm achieved in this work. The wire cross section exhibits relatively rectangular, reflecting the original shape of the fin. Fig. 5 shows the transfer characteristics of the 23nm wide nanowire device with a gate length of 350nm. In typical TFT devices, the subthreshold swing (SS) is usually beyond 200mV/dec. However, this GAA nanowire TFT SONOS device exhibits SS of 122mV/dec, which is significantly reduced compared to other reported TFT devices. Enhanced gate controllability from GAA structure is one reason to obtain such good SS, and the reduced number of grain in the nanowire channel also accounts for the good device performance. The cumulative distribution of SS for three nanowire devices with different wire widths is plotted in Fig. 6. As the wire width decreases, improved SS can be achieved, indicating the smaller wire width is favored in nanowire memory devices.

FN tunneling scheme is employed for programming and erasing (P/E) the memory cell. Fig. 7 and Fig. 8 show the P/E characteristics of a TFT SONOS cell (L_g=0.35μm). Despite 5nm thick tunnel oxide, the poly-Si nanowire memory device exhibits high memory speed than conventional planar TFT memories. For the device with 23nm wire width, the threshold voltage shift (ΔV_{th}) is 3V for a program time of only 1μs at 15V. The erase time is about 1ms at -16V to get the same ΔV_{th}. Fig. 9 compares the memory speed for devices with different wire dimensions. As programmed for 1μs, the device with smallest wire width shows the largest ΔV_{th}. The reason for the enhanced memory speed in device with smaller wire dimension could be attributed to the GAA nanowire structure. With the same stress voltage, device with smaller wire dimension exhibits larger vertical electric field across the tunnel oxide since the interface is closer to the centre [5], which could promotes larger number of carriers tunneling into the nitride trap layer. On the other hand, the enhanced electric field intensifies the conduction band bending when the device is being stressed, as shown in Fig. 10. With the larger band bending, the carrier experiences shorter barrier width to tunnel through and thus faster memory speed is observed.

To study the feasibility of MLC application, we plot the I_d-V_g at various data states in Fig. 11. Extrapolated room temperature retention for each V_{th} level is shown in Fig. 12, with the most severe degradation of only 12% after 10 years (Bit 00 to Bit 01). Fig 13 illustrates the endurance properties with a slight window closure. Table 1 benchmarks the device characteristics of The GAA nanowire TFT SONOS with other reported TFT SONOS devices.

4. CONCLUSION

In this work, GAA poly-Si nanowire TFT SONOS nonvolatile memory with minimum wire width of 23nm is demonstrated. Results reveal much improved device subthreshold characteristics and excellent device uniformity. Due to gate-all-around structure, fast P/E speed is achieved. The demonstrated large memory window enables its success for MLC applications. Therefore, the GAA nanowire TFT SONOS holds great promises for future TFT nonvolatile memory application.

References

[1] A. J. Walker *et al.*, Symp. VLSI Tech. p. 29, 2003. [2] S. C. Chen *et al.*, Appl. Phys. Lett., vol 91, p. 213101, 2007. [3] Yamauchi *et al.*, IEEE. Trans. Electron Devices, vol. 38 p. 55, 1991. [4] M. Im *et al.*, IEEE Electron Device Lett., vol. 29, p. 102, 2008. [5] J. Fu *et al.*, IEEE Electron Device Lett., vol. 29, p. 518, 2008.

- 600Å poly-Si deposition on field oxide
- α-Si fin pattern and etch
- Nanowire formation:
  steam oxidation at 730ºC. After that, nanowire is released in DHF
- ONO stack deposition (5nm/15nm/11nm)
- Gate electrode formation
- S/D formation (580ºC, 24hrs)
- Contact hole etch and metallization

Fig.1 Simplified process flow.

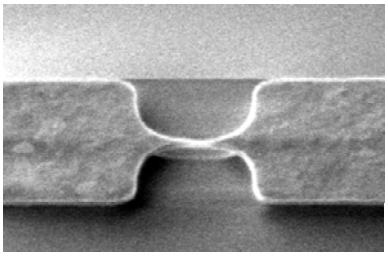

Fig.3 Tilted SEM image of poly-Si nanowire with 0.5μm long. The device fabricated has gate length of 0.35μm.

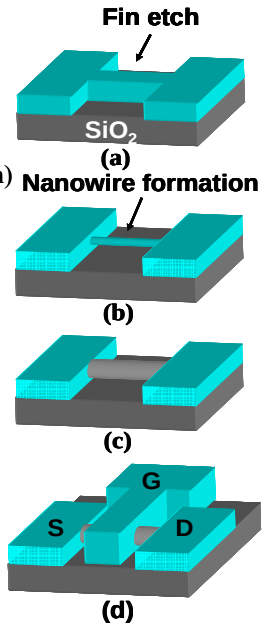

Fig.2 Schematic diagrams of main steps. (a) After fin etch (b) Nanowire formation (c) ONO stack deposition and (d) Gate electrode formation.

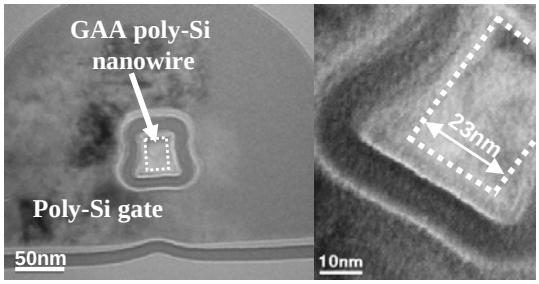

Fig.4 TEM image of poly-Si nanowire TFT device. The width of nanowire is 23nm, and the thickness for ONO gate stack is 5nm/15nm/11nm, respectively.

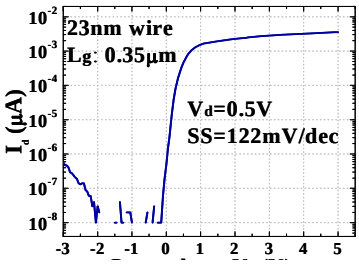

Fig.5 Transfer characteristics of poly-Si nanowire TFT SONOS. It exhibits improved SS.

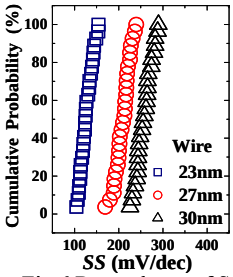

Fig.6 Dependence of SS on nanowire width. The smaller the width, the better SS.

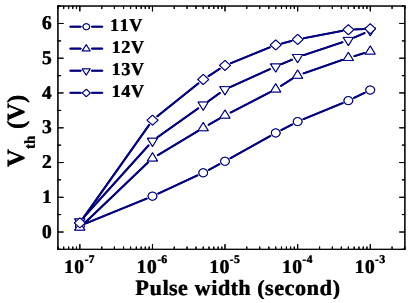

Fig.7 Program characteristic of nanowire TFT SONOS with wire width 23nm. The stressing voltage was sing from 11V to 15V.

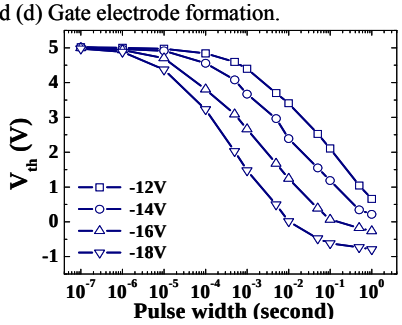

Fig.8 Erase characteristic of nanowire TFT SONOS with wire width 23nm. The stressing voltage was using from -12V to -20V.

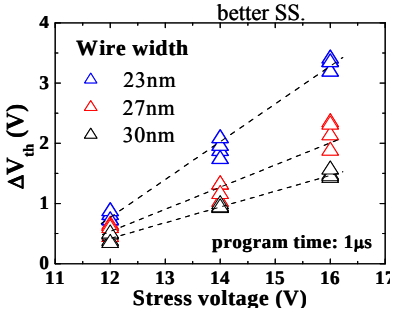

Fig.9 Comparison of memory window of devices of three wire widths under different stress voltage for a program time of 1μs.

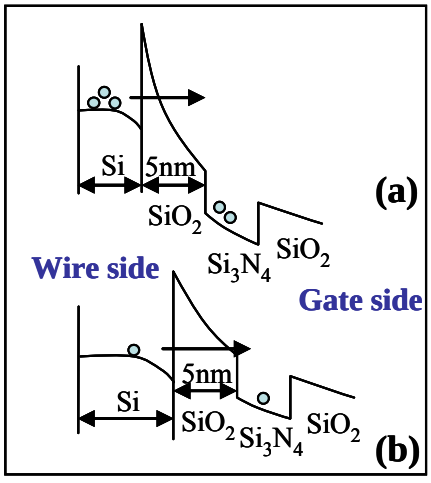

Fig.10 The band diagram during program in (a) smaller wire width device (b) larger wire width device. Stressed at same voltage, the electric field across the tunnel oxide of device with smaller wire width is larger than that of device with larger wire width, due to the particular GAA structure.

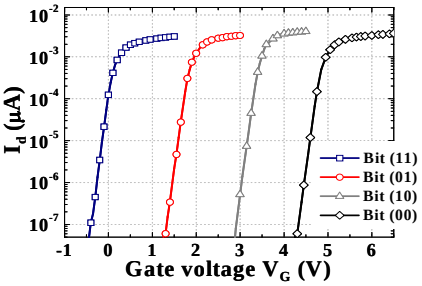

Fig.11 Plot of I_d-V_g for data states, with ~1.5V window for each state.

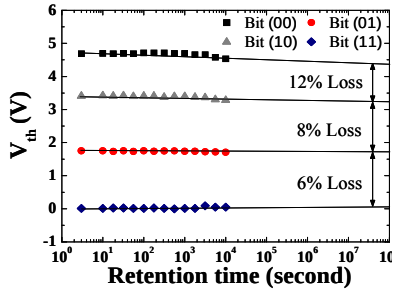

Fig.12 Retention for different data states. Bit (11) was erased back from Bit (00).

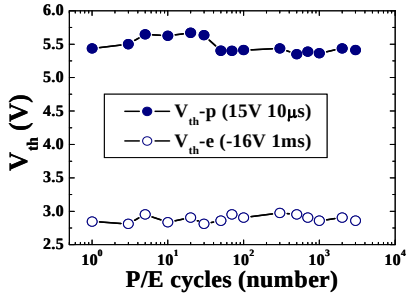

Fig.13 Endurance characteristic of nanowire TFT SONOS device.

Table 1 Comparison of TFT SONOS device

Ref.	VLSI [1]	APL [2]	This work
O/N/O	2.5/7/5nm	15/20/25nm	5/15/11nm
L/W	0.25μm technoloy	1μm/65nm	0.35μm/23nm
SS (mV/dec)	260	720	122
P/E ΔV_{th}=3V	13V,10μs/ -11.5V,10ms	25V,20ms/ -30V,100ms	13V,10μs/ -16V,3ms