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Multi-Gate Metal Nano-crystal Memories with TiN Nano-crystals, High-k Blocking Dielectric and High Work Function Gate Electrode

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Abstract

This paper presents the charge trapping layer (CTL) engineering of n-channel multi-gate FET (MuGFET) TiN nano-crystal (NC) non-volatile memory with p^+ poly-Si gate and Al_2O_3 blocking dielectric layer. After optimizing the TiN nano-laminate, large memory window of about 5.2V, good retention of 8 % charge loss after 10^4 s, and high endurance of 7 % degradation after 10^4 P/E cycles are exhibited. Multi-level operation is also demonstrated. Furthermore, a new mechanism is proposed to explain the fast retention degradation.

Introduction

As the NAND flash technology scales down continuously, the memory window and retention performance become great issues. MuGFET structure [1, 2] has been reported as a candidate for the future high density non-volatile memory. Multi-level operation was also acknowledged to be one of the solutions to increase the storage density [1]. Recently, metal nano-crystal (NC) memories were reported to exhibit better retention performance than the other NC memories [3, 4].

In this work, n-channel MuGFET TiN NC memory using p^+ poly-Si gate and Al_2O_3 high-k blocking dielectric layer is demonstrated to exhibit large memory window which can achieve multi-level operation. Furthermore, good retention performance and high endurance can also be obtained.

Device Fabrication

Fig. 1 shows the main process flow of the n-channel MuGFET NC memory on SOI wafer. The detail of each process step has been mentioned in [5]. The CTL consisting of TiN/Al_2O_3 nano-laminates with various thickness ratios and various periods were deposited and Al_2O_3 was deposited as blocking dielectric in an ALD system followed by poly-Si gate deposition. Post deposition annealing (PDA) was performed to form TiN NCs. The detailed analysis of the TiN NCs has been reported in [6]. The poly-Si gate was heavily doped to p-type. Samples with different process conditions are listed in Table 1.

Results and Dicussions

Fig. 2 shows the TEM images of the fabricated MuGFET (sample B) with gate length of 80 nm and fin width of 50nm. The high resolution image in Fig.2(c) shows tiny TiN NCs with diameter in the rage of 1~2 nm. Fig. 3 shows the transfer characteristics of sample A with different program/erase (P/E) condition. The memory window can be as large as 5.2V after P/E at ±10V for 0.1 sec. Moreover, multi-level operation can also be achieved by applying different P/E biases. Fig. 4 compares the memory window of samples A-D. The largest memory window is obtained in sample A owing to the thicker TiN (0.7nm) in the nano-laminate CTL. After PDA, NCs of sample A can be formed with diameter larger than 2nm so that more charges can be stored. The memory window of samples B-D increases monotonically with the P/E bias. However, the memory window of sample A increases to a largest value at 10V and then turn-down as the P/E bias increases furthermore. Because samples B-D do not exhibit the memory window turn-down phenomenon, the observation in sample A can not be explained by the back injection effect. Therefore, it is postulated that the stored charges enhance the electric field in blocking dielectric so that some charges loss at higher P/E bias. In samples B-D, sample B shows larger memory window presumably because the longer PDA time results in larger NCs.

Fig. 5 and Fig. 6 show the P/E characteristics of sample A-D. Sample A has the largest V_{th} shift at the same P/E time so that faster P/E speed can be used to obtain the same memory window. Because the high work function p^+ gate can restrain the back injection effect, the erase speed is faster than the program speed. Fig. 7 shows the retention performance of sample A. The charge loss is only 8 % after 10^4s and 16% after 10 years. This performance is much better than that of samples B-D as shown in Fig.8. Moreover, sample D has the worst retention property due to the thinnest blocking dielectric thickness. Fig.9 shows the endurance characteristic of sample A. The memory window is kept at 93% after 10^4 P/E cycles which is much superior to the planar NCMs owing to the electric field cancellation in MuGFET [1, 7]. Minimal degradation of S.S. and drive current after 10^4 P/E cycles is shown in Fig.10.

Fig.11 shows the retention characteristic of sample B. The retention property degrades more seriously after 10^3 s. Because the stored charges in the NCs induce strong inner electrical field, this status is similar to the constant voltage stress (CVS) on tunneling oxide and blocking dielectric. The inset in Fig.11 shows the gate leakage current (I_g) of sample B with CVS at 12V. A sudden increase of I_g after stressing for 10^3 s is consistent with the retention performance. It is proposed that the inner field due to stored charge may induce local soft-breakdown of the tunneling oxide to degrade the retention performance.

Conclusions

In this work, the effects of CTL on n-channel MuGFET TiN NC memory with Al_2O_3 blocking dielectric and p^+ poly-Si gate are presented. Device with thicker TiN in nano-laminate CTL has larger memory window, better retention, and higher endurance. Multi-level operation can be achieved with different bias conditions. New mechanism for retention degradation is also proposed.

References

[1] M. Specht, et al., IEDM Tech. Dig., p.1083, 2004.
[2] Y. J. Ahn, et al., VLSI Tech. Dig., p.88, 2006.
[3] Z. Liu, et al., IEEE TED., p.1614, 2002.
[4] J. J. Lee, et al., IEEE TED., p.507, 2005.
[5] C. P. Lu, et al., Int'l Symp. VLSI-TSA., p. 62, 2008.
[6] S. Maikap, et al., IEDMS Tech. Dig., 2006.
[7] C. P. Lin, et al., IEEE EDL., p.185, 2005.

Table.1 Gate stack structures for this study.

Sample	Tunneling Oxide: SiO_2	TiN/ Al_2O_3 (7 periods)	Al_2O_3	PDA
A	4 nm	0.7 nm/1 nm	20 nm	10 s
B	4 nm	0.5 nm/1 nm	20 nm	40 s
C	4 nm	0.5 nm/1 nm	20 nm	10 s
D	4 nm	0.5 nm/1 nm	15 nm	10 s

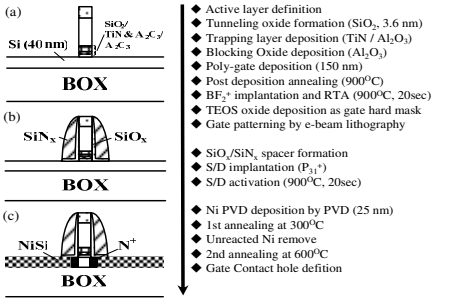

Fig. 1 Process flow of the n-MuGFET TiN NCM devices with high work function p^+ poly-Si gate (sample A).

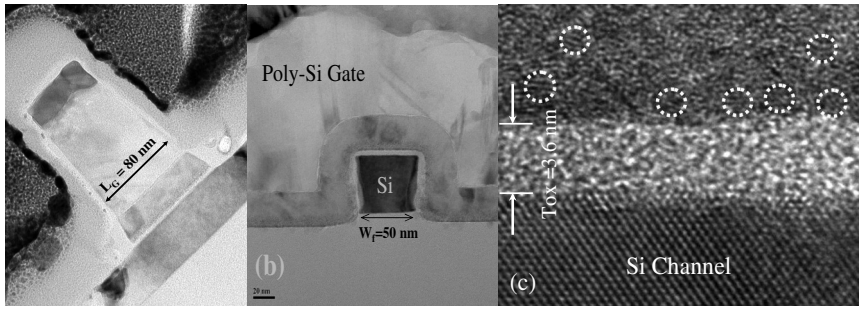

Fig. 2 TEM image of MuGFET structure with (a)gate length of 80 nm; (b) Fin Width of 50 nm; (c) NCs with diameter of 1~2nm were embedded by Al_2O_3 which has potential for future NCM application as technology scaling down.

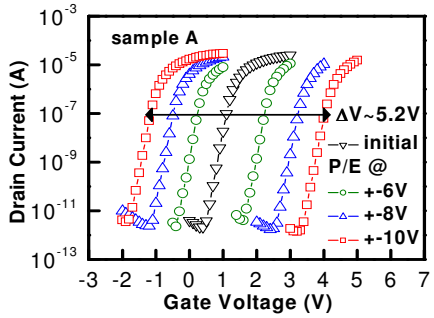

Fig. 3 Transfer characteristics of sample A at V_{ds}=1 V with different program/erase bias for 0.1 sec. Multi-level operation can be achieved.

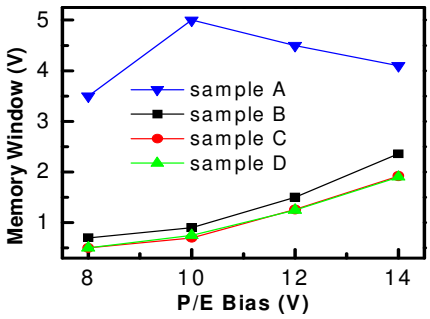

Fig. 4 Memory windows of sample A-D. Larger window is obtained by thicker TiN nano-laminate (sample A).

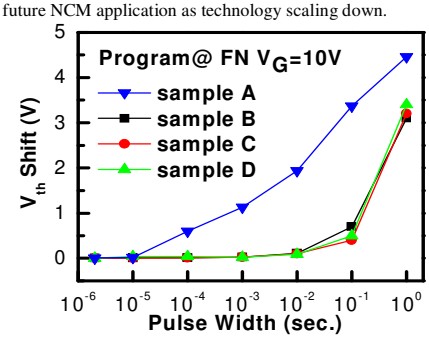

Fig. 5 Program characteristics under FN injection of sample A-D with different pulse width.

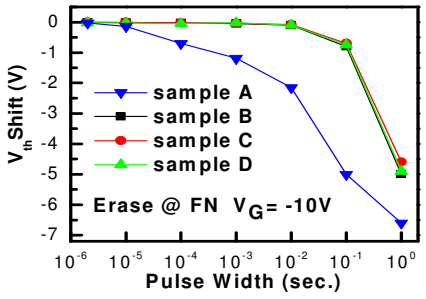

Fig. 6 Erase characteristics under FN injection of sample A-D with different pulse width.

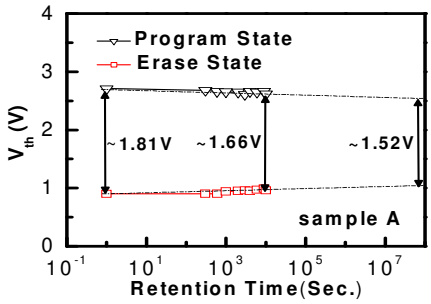

Fig. 7 Retention characteristics of sample A at 25°C. Only 16 % charge loss after 10 years.

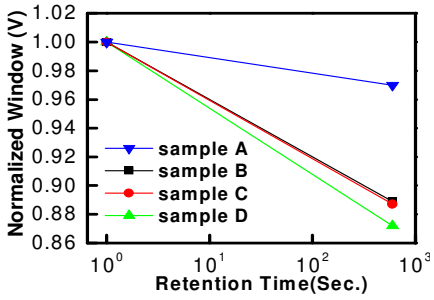

Fig. 8 Retention characteristics of sample A-D. Only 2 % charge loss after 10^3 sec. of sample A.

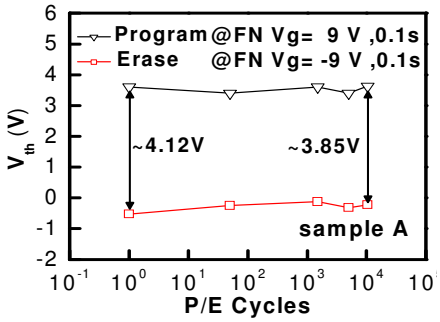

Fig. 9 Endurance characteristics of sample A shows only 8 % memory window loss after 10^4 P/E cycles.

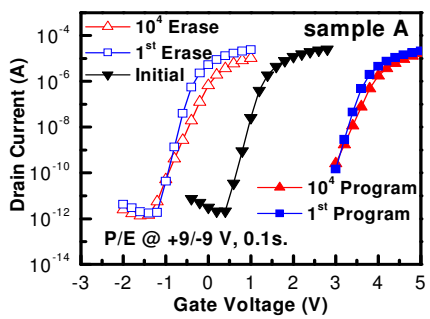

Fig. 10 Transfer characteristics of sample A reveals slight oxide degradation after 10^4 P/E cycles.

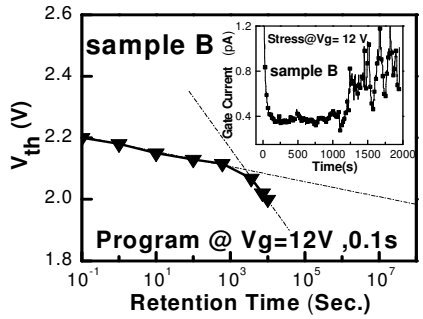

Fig. 11 Gate current of sample B with bias stress at 12V shows degradation after 1000 sec.