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A Low Voltage Programming Scheme Feasible for 2-Bit Operation of SONOS Flash Memory with Excellent Data Retention

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Abstract- A low voltage operation scheme feasible for 2-bit operation has been proposed for SONOS flash memory. First, the programming is achieved by a forward-bias assisted electron injection (FBEI), which can be used to program the 2-bits with a higher speed by comparing to the conventional Channel Hot Electron Injection (CHEI) scheme. A low voltage (~6V) at a medium speed (~1msec) can be achieved. A 2 bit/cell operation is then demonstrated, in which very good retention can be achieved, comparing to conventional CHEI operation scheme.

Introduction- In a SONOS cell, the program/erase operation is achieved via the tunneling of electrons/holes through the **very thin** tunnel oxide. Conventional operation (programming) schemes, e.g., CHEI [1] or BTB (Band-to-Band) tunneling [2], is commonly used for the programming of a 2-bit cells. However, these schemes will increase the oxide damage and then give rise to the poor retention. As a consequence, further efforts need to be developed for improving the SONOS cell retention characteristics. For example, the tunnel oxide should be thick enough to overcome the data retention problem. However, thicker bottom oxide increases the difficulty for electron injection during programming, especially in 2-bit applications.

In this paper, an improved programming scheme with forward-bias assisted electron injection scheme has been proposed, which is applicable for 1bit/cell or 2bit/cell operation. In two-bit applications, FBEI shows faster programming speed and better data retention by keeping a thick enough tunnel oxide.

1. Device Preparation

The n-channel flash cells with ONO thickness (50/60/50) (A^o), W/L=0.2/0.22(um), were fabricated using standard 0.13um CMOS technology. Medium-doped n^+-region in the S/D extension was used to maintain a high breakdown voltage.

2. Operation Schemes

Programming Scheme- For electron injection, as shown in Fig.1, called forward-bias assisted electron injection (**FBEI**), similar to **PASHEI** in [3] but with further improvement was developed. Initially, the source is floating, and the drain, gate and bulk are grounded. During time T_1, a negative voltage is applied at the drain or source, depending on where electrons are generated. During time T_2, both gate and drain (or source) are switched to positive bias, then, electrons are accelerated toward the drain (or source) and reach the nitride layer via the vertical field.

Erase scheme- A specific configuration with both source and drain tied together and by applying a higher voltage between S/D and gate will perform the injection of holes into the nitride layer, as shown in Fig. 2 with the so-called BBHI which can erase the cells to the low state.

3. Applications to 2Bit/cell Operation

Fig. 3 shows the extraction of V_T profile by the CP technique [4]-[5] along the channel. It shows the distribution which we can see the FBEI programmed charges are much closer to the drain in comparison to the CHEI programming. The I-V plot after CHEI and FBEI programming are shown in Fig. 4. As we can see, the window utilizing FBEI is larger than that of CHEI in region 2. Again, this is due to the programmed charges by FBEI are closer to the drain as shown in Fig. 3. Moreover, with high drain voltages, we will see more serious GIDL effect in Region 1 which implies FBEI charge density is higher than CHEI [6]. Fig. 5 shows the bit-2 transient for FBEI and CHEI after bit-1 is programmed. Although CHEI has faster bit-1 programming speed, longer bit-2 programming time (~10m sec) is needed. Furthermore, using FBEI programming, it only needs ~1m sec reaching to the same high state as bit-1. In other words, shorter time is needed using FBEI to program bit-2, compared to CHEI programming. The physical mechanism why CHEI needs more programming time than FBEI shown in Fig. 5 is that the trapped charges at bit-1 will affect the charge inversion and acceleration in the channel near the drain side, such that the CHEI bit-2 programming time is longer. Furthermore, in Fig. 6, this mechanism proves again that 1ms FBEI programming time for bit-2 is still unchanged even if bit-1 is programmed by CHEI. Fig. 7 shows V_T as a function of V_{read}, where a smaller V_{read} is needed for FBEI to reach 1V window at the state of programmed bit-1 and erased bit-2. This is because the charge distribution is very different between FBEI and CHEI. In Fig. 4, FBEI shows more localized distribution near the drain side than CHEI, hence a small V_{read} is needed to separate the window of programmed bit-1 and bit-2.

4. Endurance and Retention of 2-bit Operation

In Fig. 8, it shows the operation conditions of both FBEI and CHEI programming, in which BBHI are used for the erase. The cycling characteristics are shown in Fig. 9 and Fig. 10 CHEI and FBEI, respectively, in which good endurance behavior is achieved. Both the cells, in Figs.9 and 10, are programmed with 1msec and the cycle sequence is program bit-1 => program bit-2 => erase bit-1 and bit-2 together, as shown in Fig.2. The data retention after cycling is shown in Figs. 11 and 12, where an acceptable value of the four different states is achieved after 10 years. The retentions of cell programmed by CHEI and FBEI are shown in Figs. 11-12, respectively, in which better retention is achieved for FBEI. As we can see, FBEI still has 1V window after ten years in Fig. 12 which is larger than the window of CHEI retention (~0.5V) in Fig. 11. More importantly, from the data retention behavior, it shows that less damage is incurred using the FBEI scheme.

In summary, a low voltage operation scheme has been demonstrated for SONOS flash memory two bits applications. For 2bits/cell operation, the charge storage in FBEI is more localized, from the charge pumping analysis, such that this new scheme shows much better retention and endurance comparing to the CHEI ones. Moreover, smaller V_{read} lowers the power consumption and the read disturb issue can be reduced during the long term reading.

References

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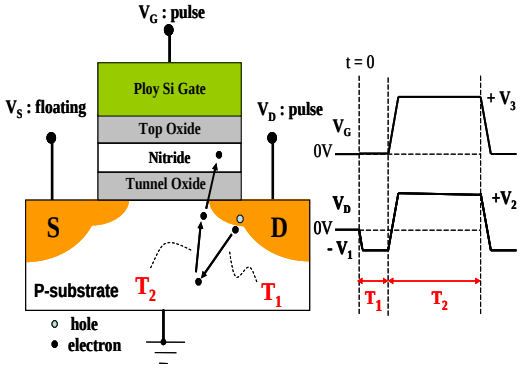

Fig. 1 Experimental set up and timing diagram for FBEI (forward-bias assisted electron injection).

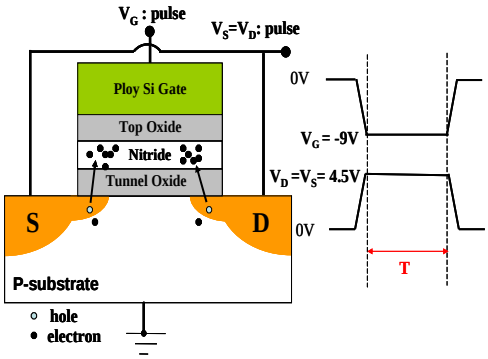

Fig. 2 Experimental set up and timing diagram for BBHI (band-to-band hot hole injection). With both source and drain are tied up together.

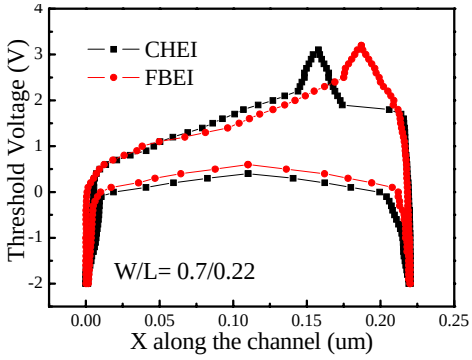

Fig. 3 The V_T distributions of one bit for FBEI and CHEI. As shown, along the channel, FBEI V_T peak is closer to the drain than CHEI.

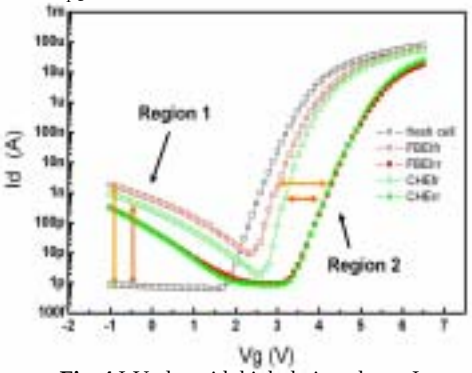

Fig. 4 I-V plot with high drain voltage. It shows that FBEI has a larger window in region 2 and higher GIDL in region 1 than those of CHEI.

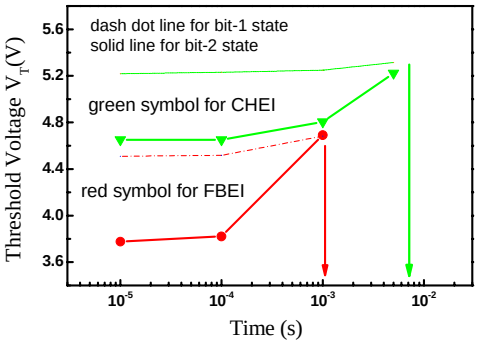

Fig. 5 The bit-2 transient for FBEI and CHEI after bit-1 is programmed. We can observe that bit-2 programmed by FBEI can reach the same threshold voltage as bit-1 in shorter time compared to CHEI.

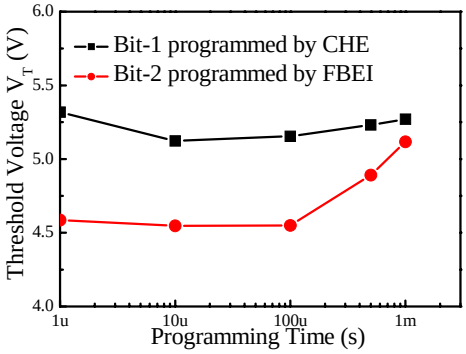

Fig. 6 The programming speed for bit-2 by FBEI while bit-1 has been programmed by CHEI. It is found that 1m sec FBEI programming time is still unchanged.

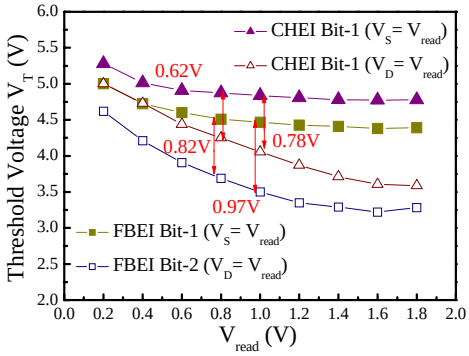

Fig. 7 V_T as a function of V_{read} .A larger window can be obtained by FBEI with smaller V_{read}.

	Program time	V_g	V_d
CHEI	1m sec	6 V	4.5 V
FBEI	1m sec	V_3=6 V	V_2=4.5 V V_1= -1 V
BBHI	10m sec	-9 V	4.5 V

Fig. 8 The operation conditions for P/E cycle with FBEI programming, CHEI programming ,and BBHI erasing in different biases and programming time.

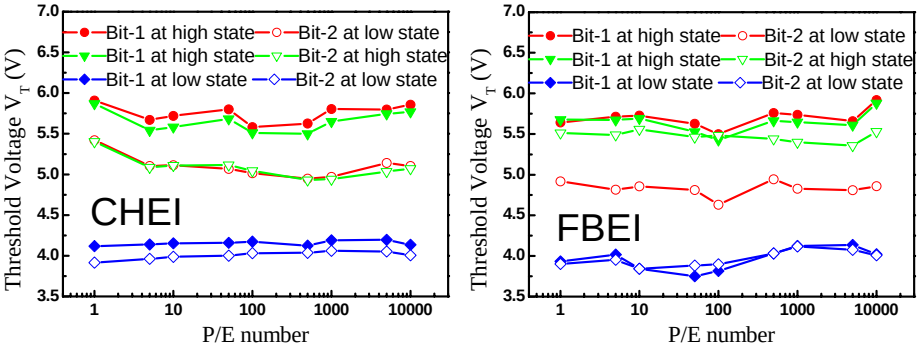

Fig. 9 and **Fig.10** Endurance characteristics of two-bit-per-cell application using CHEI and FBEI programming , respectively . Both illustrations are programmed with 1msec and the cycle sequence is program bit-1 => program bit-2 => erase bit-1 and bit-2 together.

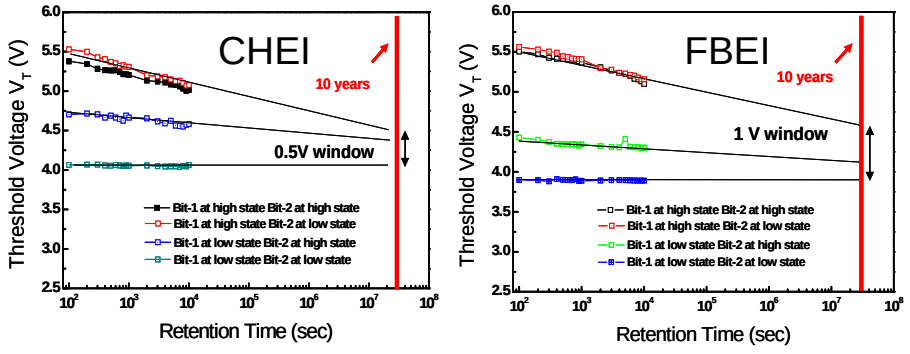

Fig.11 and **Fig.12** are the retention behaviors after 10k P/E cycles of Bit-1 and Bit-2 in four different states. The programming mechanisms are CHEI and FBEI , respectively. Obviously, with the use of FBEI program scheme, we can still achieve at least 1V window after 10 years.