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A new embedded NVM thin film cell for low voltage applications

G. Bossu[1,2], A. Demolliens[2,3], S. Puget[1,2], P.Masson[4], J-M. Portal[2], R.Bouchakour[2], P.Mazoyer[1], T.Skotnicki[1]

[1] STMicroelectronics, 850, rue Jean Monnet, 38926 CROLLES, France
2 IM2NP (UMR6242), Technopôle de Château – Gombert, 13451 MARSEILLE Cedex, France
[3] STMicroelectronics, ZI Rousset, BP2, 13106 ROUSSET Cedex, France
[4] LEAT, Université de Nice-Sophia Antipolis, CNRS 250, rue Albert Einstein, 06560 VALBONNE, France
Email : germain.bossu@st.com

Abstract

Low voltage Non-Volatile-Memories (NVM) are a challenge for embedded applications. Logic device platforms go slowly but surely to thin silicon film technology. Based on an advanced CMOS device, SQeRAM cell demonstrates here for the first time its potential for embedded NVM applications. It operates with a 3V supply only. Both threshold voltage and mobility variations are the basis of its 300mV and more memory windows. This ΔVT is obtained with a density of 10^{13} trapped electrons per cm^2.

Introduction

Non-Volatile-Memories architectures are facing major technological efforts **[1]**. Proposals to solve scaling issues are focused on gate stack shrink keeping the highest control gate coupling factor. As a consequence in a near future, the floating gate should be abandoned to the profit of local trapping using nanocristals **[2]** or trapping layer such as nitride **[3]**. In addition non-volatile memories are being developed to be compatible with future thin silicon film CMOS technologies: for FinFet **[4]** and Silicon-On-Nothing (SON) architectures **[5] [6]**. SQeRAM (SON based Quasi-non-volatile RAM) architecture has been proposed for low voltage non-volatile memory cell to address embedded NVM needs **[7]**. Electrical behavior of this cell is summarized in the following after a short description of process and morphology.

Process and Technology

SQeRAM process is described Figure 1. A double-epitaxy of SiGe and Si is performed on a bulk substrate. A gate stack is realized with nitride offsets, sacrificial oxide spacers and hard mask (A). Then gate stack and thin silicon film are protected during the junction etch (B). A partial removal of SiGe creates notches, called wings, situated under the gate (C). Wings are filled with thin ONO stack and N+ in situ doped Polysilicon depositions (D). Then several anisotropic etches prepare the surfaces for the last epitaxy (E), Source and Drain regrow keeping the wings safe (F). Figure 2 is a TEM cross-section of a resulted device which has been electrically characterized.

As one can conclude, memory charges are stored under the channel. The original gate stack of the logic devices is conserved. A Thin ONO is introduced for low voltage biases. The thickness and quality of this dielectric layer determines retention of the device. PolySilicon wings allow to apply biases under channel without any additional contact.

Memory principle: electrical properties

SQeRAM operates a less than 3V supply. The biases used in this paper are summarized in Table 1. Read operation has been performed here with drain voltage of 0.1V. Figure 3 shows after a Write sweep a 300mV memory window with a maximum bias of 2.5V on the drain. Forward (FD) and Reversed (RD) Diode pulses are used to vary the stored charge. Diode bias cycling has been used to investigate the memory ability of the devices.

Figure 4 shows the typical FD/RD cycling for the 80nm long device shown Figure 2. The ΔVT observed under threshold voltage on Figure 4a) is due to stored charge. A mobility variation is observed Figure 4b) for inversion regime as already observed with traps in gate oxide by **[8]**. Initial mobility is not completely restored by FD pulse. The sub-threshold slope is slightly degradated after the first RD pulse Figure 4a). As the sub-threshold slope stays quite similar during the cycle, there is no more interface degradation after the first pulse.

States 0 and 1 are respectively defined after FD and RD pulses. Figure 5 and 6 give memory windows after FD/RD cycle for both 30Å and 50Å gate oxide devices.

In Figure 7, ΔVT memory window corresponds to the difference of gate bias applied for a same current in the device at both states. Memory window is higher for thick gate oxide under threshold due to a better charge effect as gate coupling is lower. Memory window in inversion regime is better for a 30Å oxide thickness related to mobility variation.

Memory window study

TCAD simulation is used to evaluate charge density and mobility variations for 30Å gate oxide device. Figure 8 details the simulated device. Table 2 summarizes the used parameters according TEM cross-section analysis (Figure 2). A constant surface charge density is assumed in the ONO in both wings. Mobility and charge density have been adapted to fit the curve (Figure 9). Simulation considers memory effect due to a 10^{13} e^-/cm^2 charge density. There is a 9.5 $cm^2.V^{-1}.s^{-1}$ mobility variation between states 0 and 1. A 20 $cm^2.V^{-1}.s^{-1}$ mobility degradation is observed between initial curve and state 0.

Figure 10 shows the resulting memory windows from simulation versus measurements. The behavior in inversion regime (A) is reproduced: mobility variation is a good way to explain ΔVT increase in this regime. In far sub-threshold (B) regime it is also reproduced. The small difference of sub-threshold slope between the 2 states (Figure 6) explains ΔVT increase during the transition (C).

Conclusion

More than 300mV memory window can be obtained for a density of 10^{13} electrons per cm^2. Degradation occurs in the early steps of writing. Our study has demonstrated that SQeRAM cell memory window depends on both threshold voltage and mobility variations. Reliability enhancement needs more efforts on device integration and ONO stack.

Acknowledgment:
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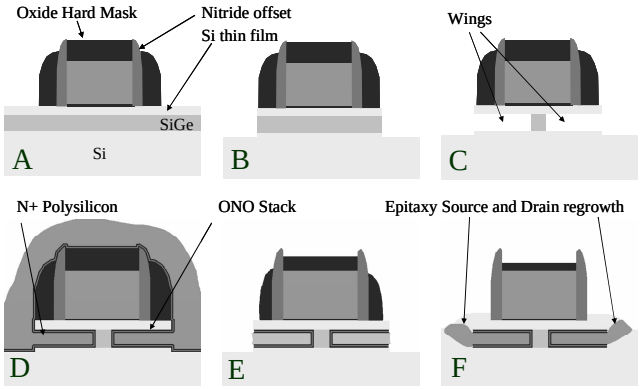


Figure 1: Specific steps of SQeRAM process technology

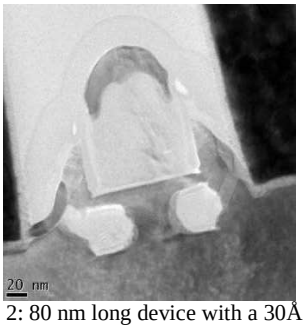


Figure 2: 80 nm long device with a 30Å gate oxide.

	VG	VS	VD	VB	duration
Read	0 V to 1.8V	0V	0.1V	0V	sweep
Write sweep	0 V to 1.8V	0V	2.5V	0V	sweep
Forward Diode (FD)	1V	-2V	-2V	0V	1s
Reverse Diode (RD)	-1V	2V	2V	0V	1s

Table 1: Used biases for our study. Low VD=0.1V for read, 2.5V for HCI.

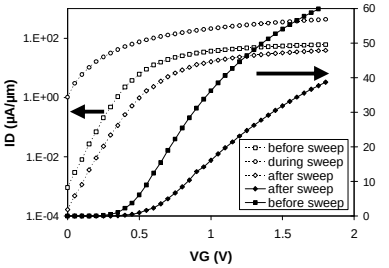
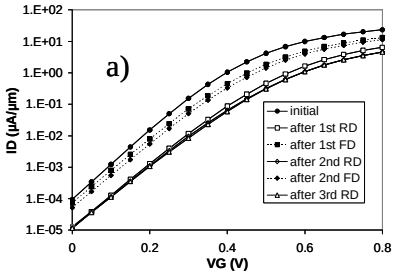


Figure 3: Read Id(Vg) VD=0.1V before and after write sweep (VD=2.5V)



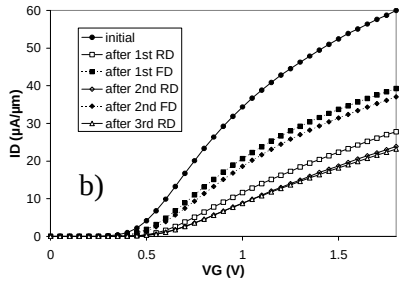


Figure 4: Read VD=0.1V Id(VG) Characteristics during Forward/Reverse Diode Cycle (FD/RD cycle) for the device shown Figure 2

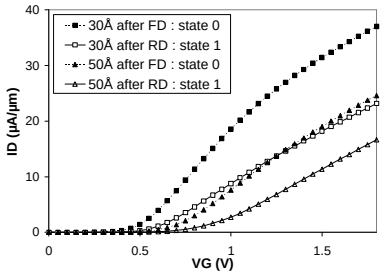


Figure 5: Read Id(Vg) with VD=0.1V after FD/RD cycle; 30Å and 50Å gate oxide

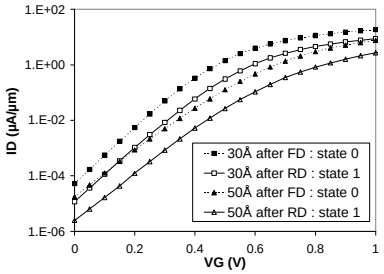


Figure 6: Read Id(Vg) with VD=0.1V after FD/RD cycle; 30Å and 50Å gate oxide

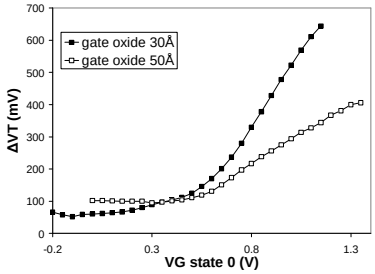


Figure 7: ΔVT memory windows for equal current among gate oxide

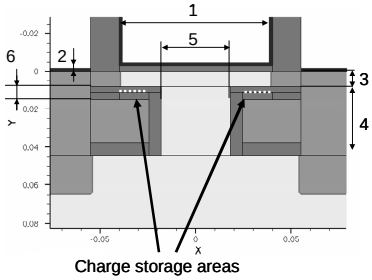


Figure 8: Simulated device overview; charge stored in the ONO of both wing

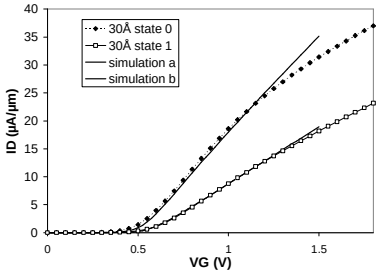


Figure 9: Measure fitting with simulation; a) 0 e^-/cm^2, µ=25 $cm^2.V^{-1}.s^{-1}$ b) 10^{13} e^-/cm^2, µ=15.5 $cm^2.V^{-1}.s^{-1}$

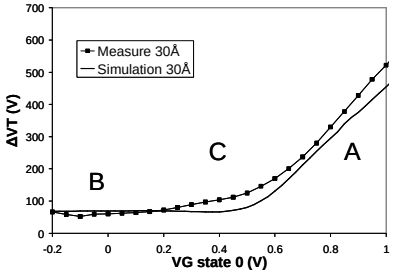


Figure 10: ΔVT memory windows comparison between measure and simulation

1	Gate length	80nm
2	Gate oxide thickness	3nm
3	Si film thickness	8nm
4	SiGe thickness	36nm
5	SiGe length	36nm
6	ONO EOT	6.5nm
Charge distance from channel		3nm
Channel Bore Doping concentration		2.10^{18} cm^{-3}

Table 2: Simulated device parameters from Figure 2 cross-section