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Enhanced Memory Performances of Advanced Impurity Trap Memory with Atomic-scale Ti Impurity Embedded in Ultrathin $LaAlO_3$ as a Charge Trap Layer

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1. Introduction

For the replacement of charge trap flash memory devices, impurity trap memory (ITM) using atomic-scale impurity charge trap layer has been developed to overcome the limitations of nitride/or nanocrystal-based charge trap memory in terms of scalability and fabrication [1-4]. However, the vertical (from impurity to Si/SiO_2 interface) diffusions of impurity degrade the electrical performance of ITM devices due to the formation of leakage paths in tunnel oxide. To form the reliable charge trap layer, these undesirable diffusions of impurity should be suppressed [5]. Thus, the advanced process development is necessary to minimize these diffusions.

In this study, atomic-scale Ti embedded in ultrathin $LaAlO_3$ (LAO/Ti) layer is introduced as a modified charge trap layer of ITM.

2. Experimentals

After standard cleaning of a p-type silicon substrate, a 35 Å of SiO_2 tunnel oxide was thermally grown at 875°C followed by the formation of atomic-scale Ti by RF sputtering (denoted by 'with Ti') in an Ar gas flow of 20 sccm at 20W. In addition, a LAO layer with the thickness of ~15 Å was deposited on some of Si/SiO_2 samples prior to Ti deposition (denoted by LAO/Ti). A 200 Å-thick Al_2O_3 blocking oxide was deposited by e-beam evaporation using single crystal Al_2O_3 source in O_2 ambient at 250°C. Post-deposition annealing (PDA) in O_2 ambient at 800 °C was performed for 1 min. For the formation of gate electrode, Pt was deposited and then conventional FGA was implemented at 400°C for 30min. Control sample is denoted by 'no Ti'.

3. Results & Discussion

To confirm the formation of atomic-scale Ti trap layer, HR-TEM analysis was performed as shown in Fig. 1. Due to the atomic-scale Ti thickness (~1.5 Å), we cannot observe the Ti trap layer in all samples. A ~15 Å-thick LAO deposited on the Si/SiO_2 sample prior to Ti deposition is also observed. Fig. 2 shows the change of capacitance after LAO deposition on the Si/SiO_2 sample. The difference of calculated EOT is approximately 2 Å. This might be due to high dielectric constant (~24) of deposited LAO layer. The memory windows (MW) of all samples are shown in Fig 3. The sample with no Ti shows negligible MW at the program/erase (P/E) voltage of 12/-10V, while with Ti and LAO/Ti samples show the large memory window of 5.2V and 5.0V, respectively. Thus, it is apparently concluded that Ti impurities play an important role to create trap sites regardless of the presence of LAO layer. P/E speed, endurance, and retention characteristics are presented in Fig. 4, Fig. 5, and Fig. 6, respectively. ITM device with Ti shows poor endurance and retention characteristic in spite of fast P/E speed. These results might be attributed to the diffusion of Ti in tunnel oxide, which causes the generation of undesirable trap states near the Si/SiO_2 interface and the reduction of tunneling distance between stored charges. Although this diffusion seems to contribute to wider MW and faster P/E operation, it leads to the significant loss of stored charges and gradual up-shift of V_{FB} during endurance characteristic, that is, MW narrowing. On the other hand, LAO/Ti sample shows superior endurance up to 10^4 cycles and 10-year retention at 85°C (MW=~2.2V). Based on these results, we propose a physical model for the understanding of improved memory performances of ITM with LAO/Ti as shown in Fig. 7. The deposited Ti atoms react with SiO_2 surface and then create charge traps. However, these atoms easily diffuse into the Si/SiO_2 interface as well as into neighbor traps during PDA [6]. On the contrary, in case of LAO/Ti sample, once stable ionic bonds are formed between Ti and LAO at LAO surface, Ti atoms may not be able to diffuse [7]. To validate this model, capacitance-time (C-t) measurement was performed as shown in Fig. 8 (a). ITM with LAO/Ti shows much longer capacitance recovery time than that of ITM with Ti, which indicates less diffusion of Ti atoms into Si/SiO_2 interface. This result is consistent with leakage current behavior as depicted in Fig. 8 (b). For further analysis, SIMS depth profiling of Ti was performed (Fig. 9). Although atomic mixing of Ti with adjacent layers is unavoidable due to the sputtering during depth profiling, the clear difference of the Ti profile between ITM with Ti and with LAO/Ti is observed. These ensure that additional LAO layer makes atomic-scale Ti reliable for impurity trap.

4. Summary

Advanced ITM device with LAO/Ti was intensively investigated. ITM with LAO/Ti trap layer shows significant improvements of endurance and retention characteristics while maintaining large MW and reasonable P/E speed because of the suppression of Ti diffusion by ultrathin LAO layer. Our approach might be promising for scaling down of the next generation nonvolatile memory.

Acknowledgments

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References

[1] Y. Yang et al., *Solid-State Electron.* **43** (1999) 2325
[2] S. Tiwari et al., *IEDM, Tech. Dig.*, (1995) 521
[3] H. Sunamura et al., *IEEE-NVSMW,* (2006) 70
[4] M. Kwon et al., *Appl. Phys. Lett.*, **90** (2007) 193512
[5] H. Sunamura et al., *IEDM, Tech. Dig.*, (2006) 975
[6] H. Dallaporta et al., *Phys. Rev. B*, **41** (1990) 5075
[7] Sreco Skapin et al., J. Am. Ceram. Soc., **76** (1993) 2359

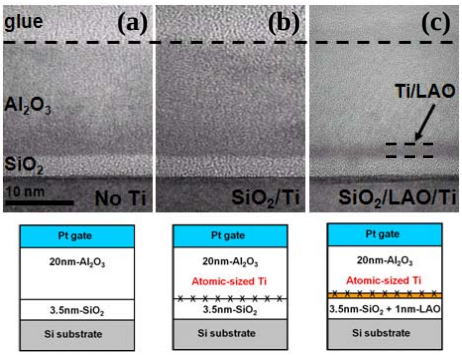

Fig. 1 Cross-sectional TEM images and schematic diagrams of ITM devices; (a) no Ti (b) with Ti (c) with LAO/Ti.

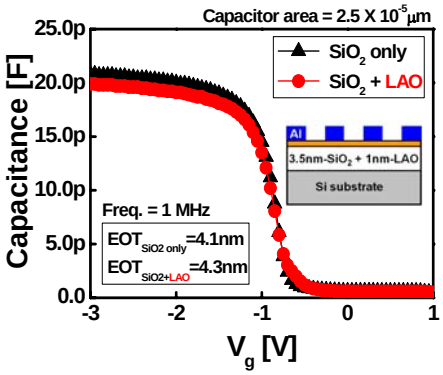

Fig. 2 High frequency C-V curves of MOS capacitors with $Si/SiO_2/Al$ stack and with $Si/SiO_2/LAO/Al$ stack. The difference of EOT is approximately 2 Å.

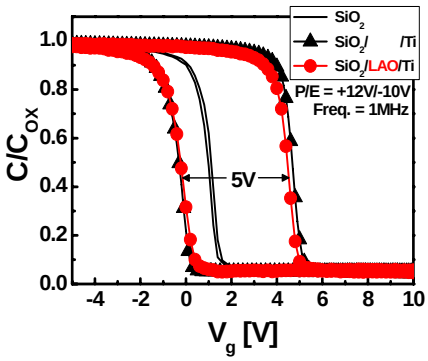

Fig. 3 High frequency C-V hysteresis curves of no Ti, with Ti, and with LAO/Ti samples.

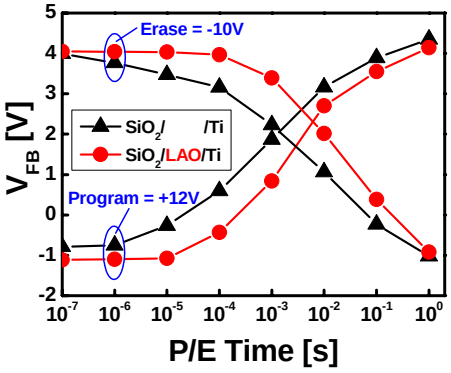

Fig. 4 P/E speed characteristic of ITM with Ti and with LAO/Ti.

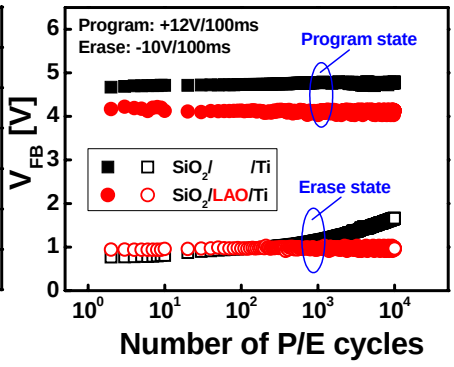

Fig. 5 Endurance characteristic of ITM with Ti and with LAO/Ti.

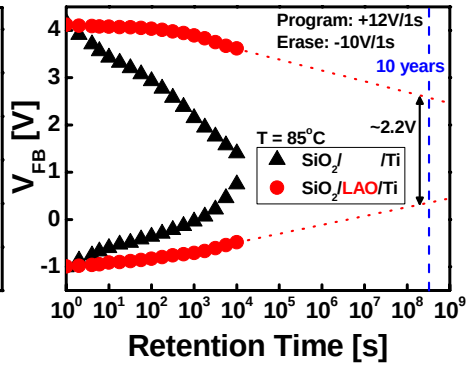

Fig. 6 Retention characteristic at 85℃ of ITM with Ti and with LAO/Ti.

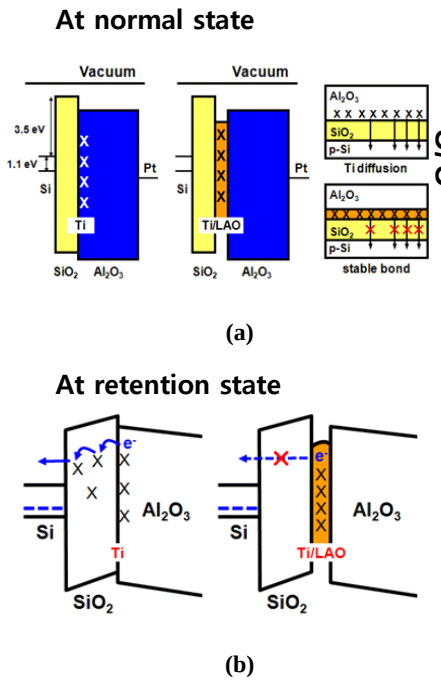

Fig. 7 The proposed physical models for the improved memory performances of ITM with LAO/Ti; (a) at normal state (b) at retention state. Ti impurities are denoted as black-colored 'X'

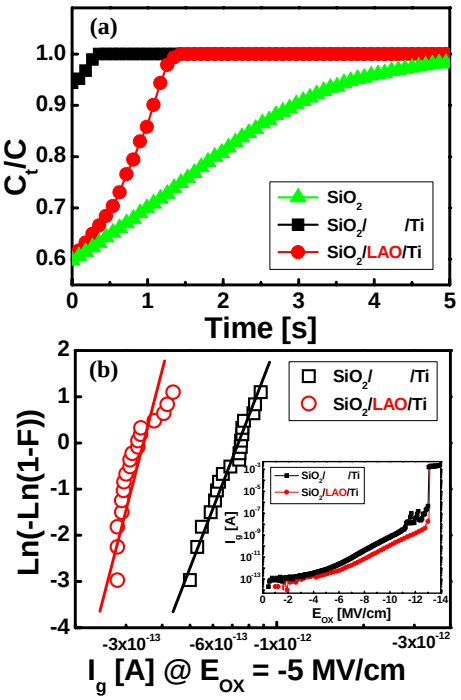

Fig. 8 C-t transient analysis (a) and Weibull plot of I_g @ E_{OX} = -5 MV/cm (20 points) (b) from the typical I_g-V_g curves of ITM with Ti and with LAO/Ti (inset of (b)).

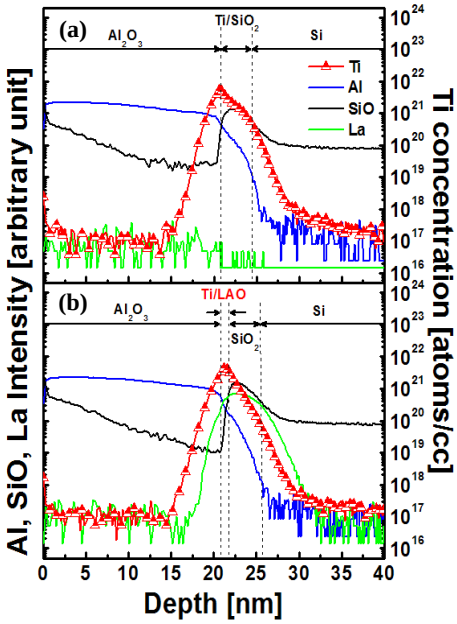

Fig. 9 SIMS depth profiles of ITM with Ti (a) and with LAO/Ti (b). The profile broadening of La is due to its much heavier atomic mass compared to that of Al, Si, and Ti.