Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 1152-1153

J-7-4

Multi-Level-Storage in Lateral SbTeN-based Phase-Change Memory with an Additional Top TiN Layer

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1. Introduction

There is a growing demand for memory nowadays. One of the most effective approaches to increase the memory capacity is the multi-level storage (MLS), by which much more information can be stored without increasing memory size. Phase-change memory (PCM) based on amorphous-crystalline transition [1-5] is expected to apply to MLS since a lot of intermediate resistance levels are possible by controlling the total crystallinity between electrodes.

However, most of today's PCMs with a single phase-change chalcogenide layer and an in-series heater exhibit sharp resistance changes with the programming pulse amplitude [1, 3], which makes them very difficult to apply to MLS in a stable and controllable way.

In order to obtain gradual (or step-like) resistance change characteristics, PCMs with stacked chalcogenide layers were proposed and they exhibited MLS potential. However, the number of storage levels depends strongly on the number of chalcogenide layers and only four-level-storage was demonstrated up to now due to the difficulty in design [6-8].

In this study, we demonstrate the possibility of MLS by using a lateral SbTeN-based structure (LTH-PCM) with the help of a top heating layer of TiN. The number of distinct resistance levels can readily reach eight and even higher, depending on programming currents.

2. Experimental

The active layers of the LTH-PCM device consist of 150-nm-thick SbTeN layer and an additional top 50-nm-thick TiN layer, as shown in the left inset of Fig. 1. The SbTeN and TiN layers were both deposited using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a sputtering pressure of 0.2 Pa. The Sb_2Te_3 and Ti targets were used. N_2 and Ar gases were simultaneously introduced into the chamber during sputtering. For the SbTeN film, gas flow rates of N_2 and Ar are 1 and 14 sccm, respectively. Amorphous and crystalline SbTeN films have resistivities of around 9×10^{1} and 4×10^{-3} Ω cm [9]. For the TiN film, gas flow rates of N_2 and Ar are 2 and 8 sccm, respectively. The TiN film has a resistivity of around 2×10^{-3} Ω cm.

Current-voltage (*I*-*V*) characteristics of the devices were measured by semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.). Device resistance was read out at a low current (e.g. 0.02 mA).

3. Results and discussion

Fig. 1 shows the programming of the device by the current sweepings from 0 to the programming currents I_p. The programming currents were 0.5, 1, 2 and 3.5 mA, respectively. The upper right inset of Fig. 1 shows the detailed sweeping *I*-*V* curves. It can be seen that the intermediate levels were very stable because the changed resistance levels can be retained until the sweeping current became higher than the former programming current. The *R*-I_p curve shows three distinct intermediate levels. This allows 5-level-storage. It should be noted that more intermediate levels are possible by reducing the programming current intervals. Fig. 2 shows the device resistance change induced by current pulses up to 1 mA in 0.1 mA increments. Here, nine distinct resistance levels were obtained.

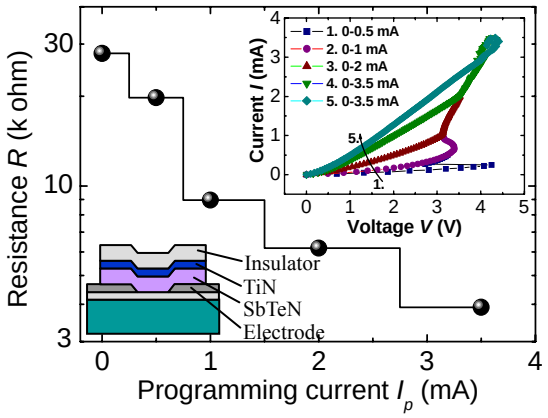

Fig. 1. A typical graph of resistance drop induced by current sweeping (Wg=700 nm; Lg=3000 nm).

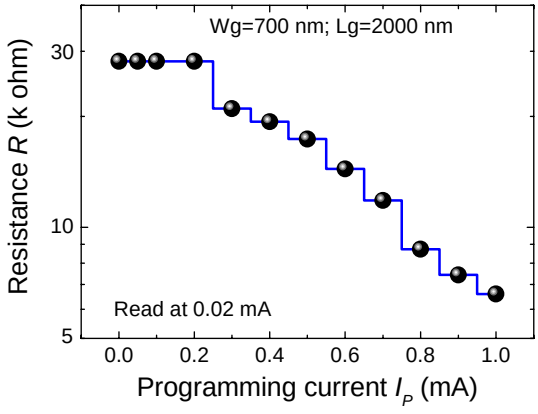

Fig. 2. Device resistance drop induced by programming current pulse.

The multi-level storage in the LTH-PCM device can be explained according to diagrams in Fig. 3. And here, we take four-level storage as an example. Device resistance R0 is the highest resistance level when the phase-change (PC) layer is totally in the amorphous phase as shown in Fig. 3(a). The equivalent circuit of the highest level is shown in Fig. 3(e). When applying increasing current to the device,

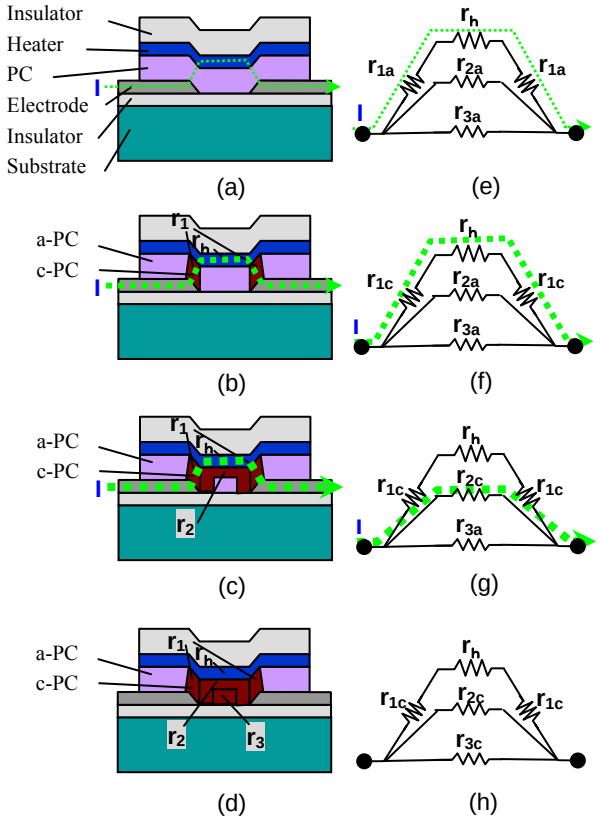

Fig. 3. Schematic diagrams of operation mechanism in LTH-PCM device. (a) High-resistance amorphous state. (b) Intermediate-resistance state with crystalline regions induced by an electric field above the threshold field. (c) and (d) Resistance state with enlarged crystalline regions driven by Joule heating. (e-h) Equivalent circuits corresponding to (a-d), respectively.

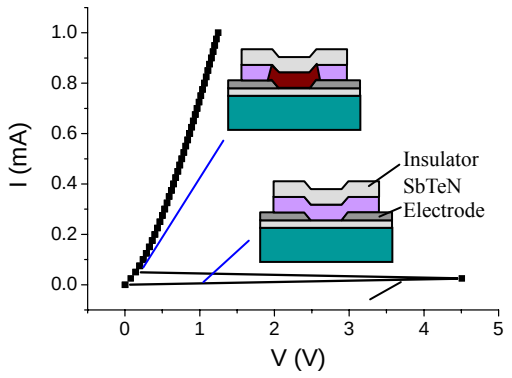

Fig. 4. No gradual switching can be observed for the device without a top heating layer.

firstly, the resistance r_1 at steps in the PC layer as shown in Fig. 3 (b) changes from r_{1a} to r_{1c} due to the high electric field at the steps. Previous experimental results revealed that the crystallization locally happened via its initial filament formation when the electric field across PC layer reached its threshold value [10, 11]. Then the current flowing through one electrode, one step of PC, the top heater, another step of PC and another electrode heats the layer surrounded by these parts. The resistance of this layer is r_2 as shown in Fig. 3 (c). As a result, r_{2a} will drop to r_{2c} due to the Joule heating. r_{2a} and r_{2c} are resistances of this layer in the amorphous and crystalline phases, respectively. Similarly, total device resistance can drop gradually through the enlargement of crystalline regions by Joule heating. Consequently, several intermediate resistance states are available.

The TiN layer plays an important role during programming in the device. It changes the current path between electrodes and facilitates the electric field concentration. The subsequent Joule heating from the TiN layer leads to the initial enlargement of the crystalline zone. The role of TiN for MLS can be known from Fig. 4. The device without a top TiN heating layer did not exhibit the gradual switching by Joule heating. Crystallization must suddenly take place when the electric field between electrodes become higher than the threshold electric field of SbTeN in the device.

4. Conclusions

A lateral phase-change memory with a top-heater (LTH-PCM) is proposed and investigated for MLS. The active layers consist of a 50-nm-thick TiN layer as a top heater and a 150-nm-thick SbTeN layer. Experimental results exhibit a number of intermediate levels are distinct and stable, which are induced by electric currents. The multi-level storage results mainly from the gradual enlargement of crystalline region between electrodes by Joule heating according to our analysis.

Acknowledgements

We would like to express thanks to financial support by STARC of Japan.

References

[1] S. Lai, et al., *Tech. Dig. IEDM* (2001) 803.
[2] Y. Yin, et al., Jpn. J. Appl. Phys. **44** (2005) 6208.
[3] A. L. Lacaita, Solid-State Electronics **50** (2006) 24.
[4] N. Matsuzaki, et al., *Tech. Dig. IEDM* Session 31.1 (2005).
[5] S. Hosaka, et al., IEEE Transactions on Electron Devices **54** (2007) 517.
[6] J. Feng, et al., Jpn. J. Appl. Phys. **46** (2007) 5724.
[7] Y. Yin, et al., Microelectron. Eng. **84** (2007) 2901.
[8] F. Rao, et al., Jpn. J. Appl. Phys. **46** (2007) L25.
[9] Y. Yin, et al., J. Appl. Phys. **102** (2007) 064503.
[10] S. R. Ovshinsky, et al., IEEE Transactions on Electron Devices **ED-20** (1973) 91.
[11] M. H. R. Lankhorst, et al., Nature Mater. **4** (2005) 347.