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Current Development Status and Future Challenges of Spin Torque Transfer MRAM Technology

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1. Introduction

Spin transfer torque RAM (SPRAM) on TMR technology is one of the promising candidates for universal memory. In this type of memory, the thermal stability factor (E/k_BT) of a TMR cell determines the nonvolatility and the current through a CMOS transistor determines the threshold current density (J_{c0}) for spin transfer torque (STT) writing. However, both E/k_BT and I_{c0} are proportional to TMR cell size. Therefore it is not easy to realize highly nonvolatile SPRAM with small write current. In this paper, we propose a TMR cell with 10-year period of data retention for SRAM-compatible nonvolatile RAM.

2. Chip specification and estimation of required E/k_BT

Figure 1 shows a photograph of the chip and the target specification for TMR cells for SRAM-compatible operation with 10-years data retention. The cell size of the is 2.56 μm^2 and is fabricated with 0.2 μm CMOS and 0.1 μm TMR technology. The maximum drivability of the cell transistor is about 500 μA.

It is well known that STT switching is the probabilistic phenomena[1], and it is essential to evaluate switching probability in ns regime in order to set the proper read and write current. Figure 2 is an example of the dependence of switching probability on the applied current density. The probability was calculated from 100 cycle measurements on each current density. When the pulse duration is more than 10 ns, which is the time region used for our SPRAM, we could fit the data using the following equation for thermal activation regime[1];

$$P = 1 - exp[-\tau_p/\tau_0 \, exp\{ -E/(k_B(T^2+\beta J^2)^{1/2}(1-J/J_{c0})\}] \quad (1)$$

where J is write current, τ_0 is the attempt time, τ_p is the pulse duration, and E, k_B, and T are the energy barrier, the Boltzmann constant, and temperature, respectively. Using this equation, we have evaluated the target value of E/k_BT. The required E/k_BT for a non-destructive read and 10-years data retention are 56 and 64 under the specification shown in Fig.1

3. SPRAM chip properties

In order to realize the specifications for both E/k_BT and J_{c0}, we used the TMR cell has a $Co_{20}Fe_{60}B_{20}$ synthetic-ferri (SyF) ferromagnetic free layer, MgO barrier layer, and a pinned layer as shown in Fig. 3 (a). The SyF free layer consists of a thin Ru spacer and two ferromagnetic layers. We fabricated TMR cells changing the thickness of one ferromagnetic layer in a SyF free layer as shown in Fig. 3 (b).

At first, we optimized E/k_BT and J_{c0} of the samples fabricated on thermal oxidized Si wafers. Figure 4 shows the dependence of E/k_BT and J_{c0} on the thickness of the upper $Co_{20}Fe_{60}B_{20}$ layer. These indicate that E/k_BT is maximum and J_{c0} is minimum when t_2 is close to t_1. Therefore, we fabricated the SPRAM chip using TMR cells with a SyF free layer with the same thickness of 2 nm. Figure 4 (a) shows the cross-sectional view of a TMR cell and Figure 4 (b) shows the relationship between switching current and pulse duration. E/k_BT and J_{c0} are evaluated to be 57 and 3.3 x 10^6 A/cm^2, respectively. Since we have confirmed that E/k_BT can be increased according to the increase in the thickness of the free layer without increasing J_{c0}[2], we can achieve an E/k_BT more than 64 and a write current less than 500 μA/cell, when the thickness of the free layer is increased to 2.5 nm.

Figure 6 shows the distribution of the resistances in both the parallel and aiti-parallel states. The mean values of the parallel resistance (R_P) and anti-parallel resistance (R_{AP}) are 1.7 kΩ and 3.3 kΩ. The resistance variations ($\pm 3\sigma$) in R_P and R_{AP} were 400 Ω and 600 Ω, respectively. These indicate that there is enough in the resistance for reading circuits to determine 'High' and 'Low' state

4. Conclusion

We developed a TMR cell for SRAM compatible nonvolatile RAM. The switching probability with pulse duration of more than 10 ns can be expressed by thermal fluctuation regime. A thick synthetic ferri ferromagnetic free layer with $Co_{20}Fe_{60}B_{20}$ can achieve an E/k_BT of 64 and cell write current of less than 500 μA.

Acknowledgements

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References

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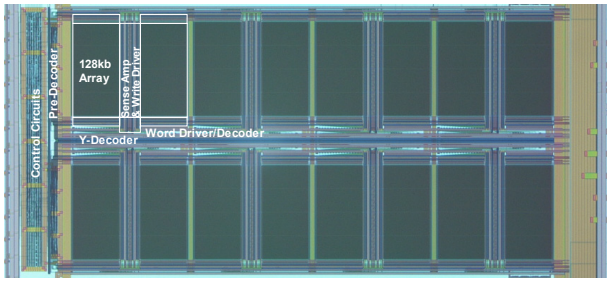

Cell size/TMR size	1.6 x 1.6 μm2 /100 x 160 nm2
Density, Vcc, Rule	2Mb, 1.8V, 0.2um
Access Time (*t*read/*t*cycle)	10 ns/30 ns
Icell(Read)/Iw(Write)	40/400uA/cell, 8 bit read
Retention time	10 years
Chip Error Rate	< a few FIT

Fig. 1 Chip photograph and specifications

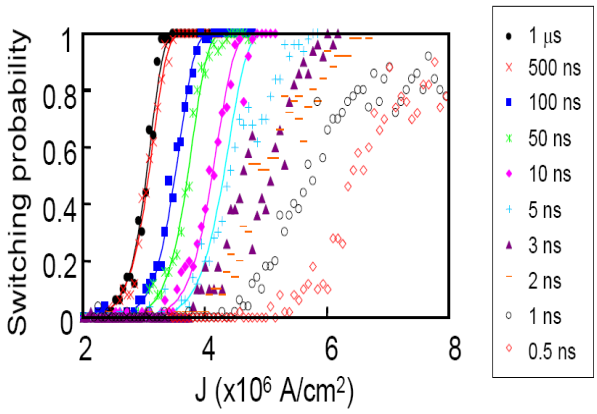

Fig.2 Current density dependence of switching probability

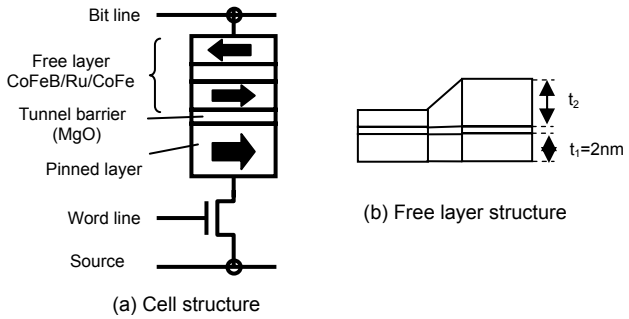

Fig. 3 Cell and TMR structure

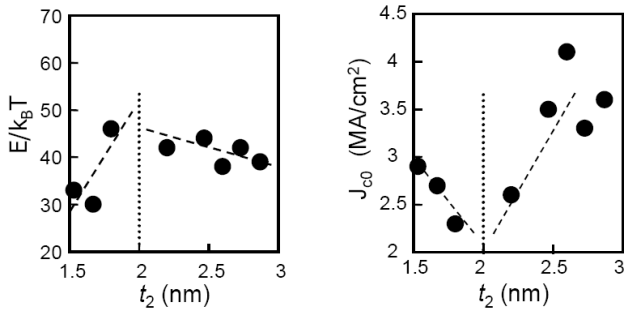

Fig.4 CoFeB thickness dependence of E/k_BT and J_{c0}

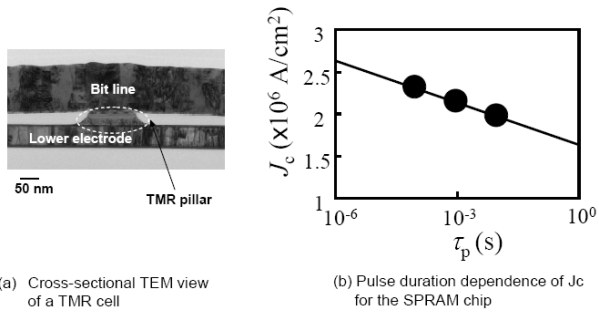

Fig. 5 TEM view of a TMR cell and pulse duration Dependence of J_c

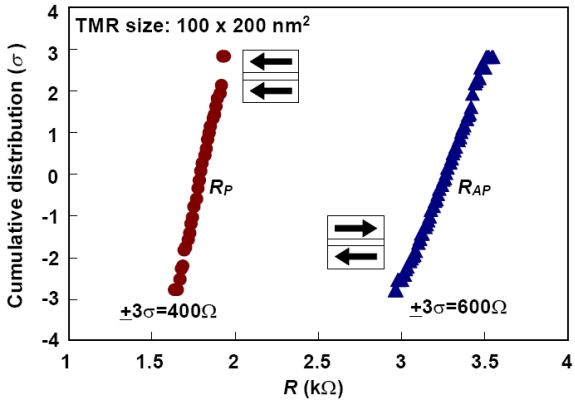

Fig. 6 Resistance distribution