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Resistive switching Ion-Plug memory for 32-nm technology node and beyond

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1. Abstract

We report a novel resistive switching Ion-Plug memory (IPM) with a dual-layered structure containing a solid electrolyte layer (supply layer) that has Cu ions and a resistive switching layer (memory layer). By adopting this structure, IPM achieved high endurance and long retention time compared to previously reported solid electrolyte memory [1, 2] because excess Cu deposition was prevented. The conductive pathway of Cu with a 20 nm ϕ was observed by cross sectional TEM. Generation/rupture of the pathway enables local resistance switching at diameters smaller than 32 nm ϕ. A set/reset operation that takes 30 ns and an endurance of 10^9 cycles were presented. IPM is a promising candidate for high-density memory for 32-nm technology node and beyond.

2. Introduction

For overcoming a serious scaling limit of dynamic random access memory (DRAM) and NAND flash memory at 32-nm technology node, a lot of memory types have been reported in recent years such as phase change memory (PCM) [3] and metal-oxide resistive memory [4]. However, these memories seem to have a critical issue of a large reset current. Another type of memory is solid electrolyte memory [1, 2], which is expected to achieve good scalability and a small current operation. However, in previous studies on memories, long retention time and high endurance were not simultaneously presented. We propose the IPM for low power consumption, high endurance, and high-capacity memory application.

3. Memory characteristics

A cross-sectional schematic of IPM is illustrated in Fig. 1. An 8-nm-thick memory layer of Cu-Ta-O, a 15-nm-thick supply layer of Cu-Ta-S, and a top electrode of W-Ti with a 300-nm thickness was deposited by RF-magnetron sputtering on bottom electrodes that were made of W and patterned to between 100 and 640 nm ϕ. The supply layer contained 51 atomic percent Cu that was confirmed by EDX. The upper electrode was biased positively with respect to the bottom electrode for set operation and biased negatively for reset operation. Typical voltage sweeping I-V and R-V characteristics of IPM are shown in Fig. 2. The arrows indicate the operational direction. The set/reset occurred at +2/-1 V with a set current of 20/80 μA respectively. The set resistance (R_L) and the reset resistance (R_H) of various devices all processed under the same conditions are shown as a function of bottom electrode size. The R_L was size independent, whereas the R_H increased with electrode size. This indicates that IPM switches in a local area are smaller than 100 nm ϕ. The local conductive pathway of Cu with a 20 nm ϕ was confirmed by cross-sectional TEM and EDX mapping of Cu in a set state, as shown in Fig. 4 (a-2, 3) and (c). The fcc crystal of Cu was verified by electron diffraction as shown in Fig. 4 (d). On the other hand, the local pathway structure of Cu was not observed in the TEM image of the reset state after a few set/reset cycles, as shown in Fig. 4 (b-2, 3). From electrical and TEM studies, the switching mechanism of IPM is illustrated as follows (schematically shown in Fig. 1): Cu ions in the supply layer migrate toward the memory layer due to an applied electric field; Cu is deposited by deoxidization of Cu ions and a local conductive pathway forms through the memory layer, and the conductive pathway is ruptured by a reverse electric field. In Fig. 5, the pulse width dependence of the switching voltage is shown at 300 and 400 K. The set and reset voltage were pulse-duration independent from 30 to 300 ns and deceased with temperature, probably due to thermal activation of Cu ion mobility. Switching at 30 ns is a sufficient rate for NAND-flash-compatible operation. The retention characteristic at room temperature is shown in Fig. 5. Even after 10^5 seconds, R_H and R_L remain constant without degradation, which indicates a potential for a 10-year retention time. The result of endurance measurements performed at room temperature is presented in Fig. 7. The set/read/reset/read cycles were repeated for 10^9 cycles without serious error.

4. Conclusion

We demonstrated Ion-Plug memory (IPM) with high endurance, long retention time, and good scalability. Resistance change occurs by generation/rupture of conductive pathways due to electro-chemical reactions of Cu. The current status of IPM compared to PCM, DRAM, and NAND flash memory is shown in Table 1. IPM has a potential to be a new nonvolatile memory from the viewpoint of endurance, retention time, and scalability. IPM exhibits good operating speed for DRAM and DRAM compatible memory from the viewpoint of writing speed.

References

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[3] Y. Matsui, *et. al.*, Ext. Abs. IEDM (2006) 769.
[4] Myoung-Jae Lee, *et. al.*, Ext. Abs. IEDM (2007) 771.

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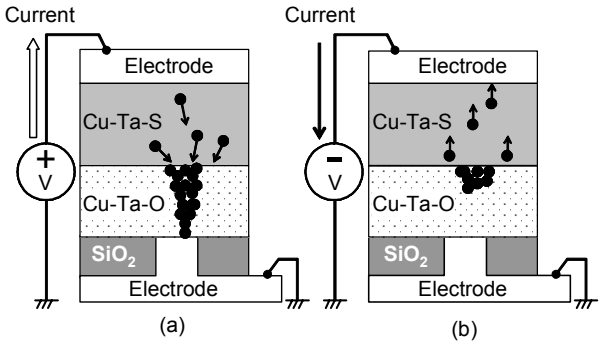

Fig. 1 Schematic of Ion-Plug memory switching mechanism. (a) Set operation. (b) Reset operation.

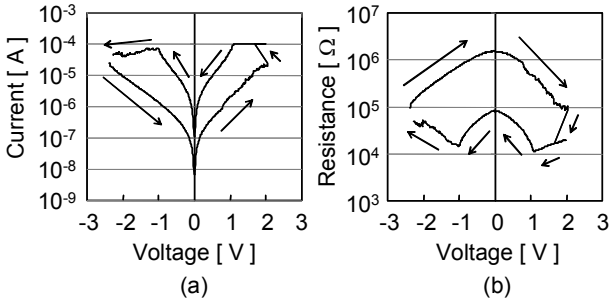

Fig. 2 Typical (a) I-V (b) R-V characteristics of Ion-Plug memory. Arrows indicate operational direction.

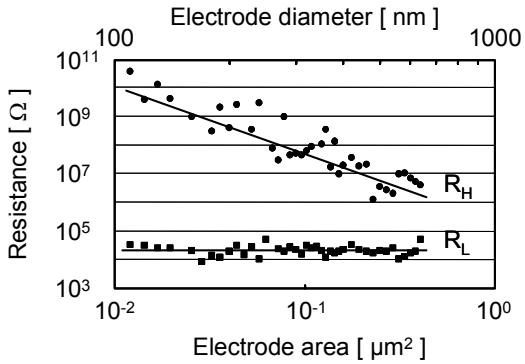

Fig. 3 Bottom electrode area dependence of resistance.

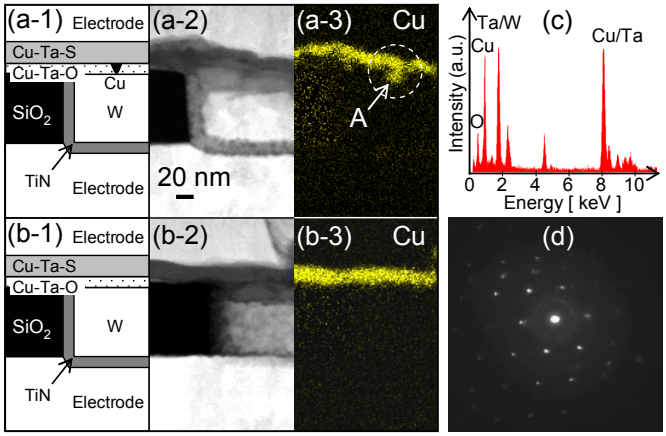

Fig. 4 (a-1) Schematic of cross section, (a-2) STEM image, and (a-3) EDX mapping of Cu in set state. (b-1) Schematic of cross section, (b-2) STEM image, and (b-3) EDX mapping of Cu in reset state. (c) EDX spectrum and (d) electron diffraction of point-A.

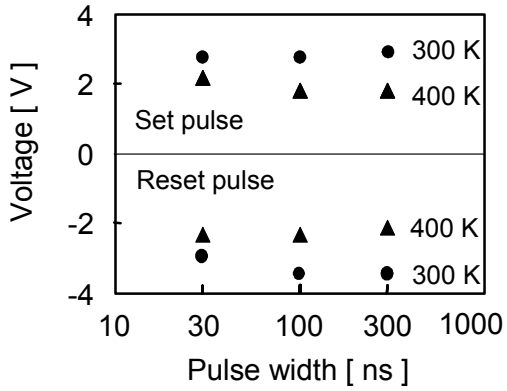

Fig. 5 Pulse-width dependence of set/reset voltage.

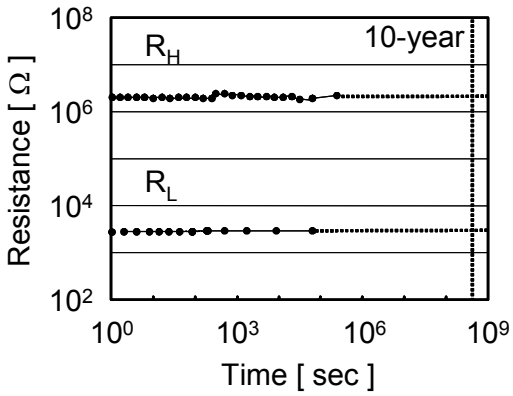

Fig. 6 Retention characteristics for set/reset state.

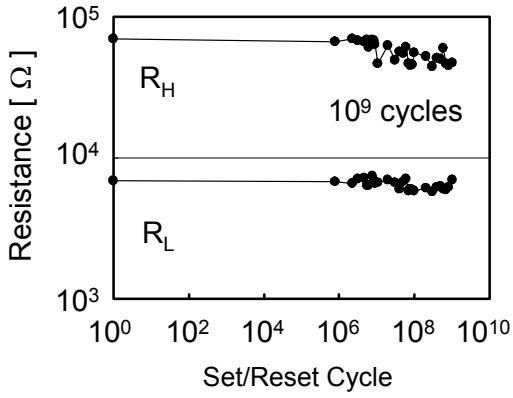

Fig. 7 Endurance characteristics of Ion-Plug memory. AC measurement without verification loop. 10^9 set/reset cycles.

Table. 1 Summary of switching characteristics of Ion-Plug memory compared to PCM, DRAM, and NAND flash.

	Ion-Plug Memory	PCM	NAND Flash	DRAM
Endurance	> 10^9	10^7	10^5	10^{16}
Write Time	< 30 ns	1 μs	200 μs	10 ns
Retention Time	> 10^5 s	10 years	10 years	< 1 s
Program Current	80 μA	100 μA	1 nA	10 μA
Write Voltage	3 V	1.5 V	20 V	1.2 V