Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 1168-1169

J-9-4

Low-Voltage and Fast-Speed Forming Process of Tungsten Oxide Resistive Memory

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1. Introduction

The concept of using resistive switching of transition metal oxides (TMO) in RRAM has attracted a lot attention because TMO is highly compatible with standard CMOS process [1-7]. Before operating the TMO based RRAM, many studies report that a forming process is necessary to initialize the resistive memory switching [1-6]. A common forming process utilizes a direct current (DC) sweeping to breakdown and activate the device from the high resistance state (HRS) to the low resistance state (LRS). In our previous work, we found that WO_x shows RRAM behavior without a forming process [7]. Although good switching characteristics are observed, a higher resistance of the device is preferred for matching the access devices. In this work, we use a low-voltage and fast-speed electrical treatment to improve the switching characteristics of the WO_x RRAM devices.

2. Device Fabrication

A schematic plot and fabrication process flow are respectively shown in Fig. 1(a) and (b). After the W-CMP process, the WO_x layer is fabricated by using a down stream plasma oxidation at 150 °C for 400 sec with an O_2:N_2 ratio of 20. The TEM microstructure of WO_x is shown in Fig. 1 (c), and the WO_x film is amorphous after processing.

3. Results and Discussion

The initial resistance of the WO_x film is about 600 ohm, compared to the high initial resistance in other metal oxides. The forming process is defined as the electrical treatment to switch the device from LRS to maximum HRS. The dependence of the resistance and the pulse voltage is shown in Fig. 2 and the maximum HRS is observed after a 3.5 V/80 ns forming pulse. Table 1 compares the forming process of different metal oxides. In most literatures, the forming process is a high voltage and slow electrical DC sweep, which increases the circuit complexity and testing time severely. In this WO_x-based device, a single pulse of 3.5 V/80 ns is capable for forming the device.

The voltage-sweeping measurements before and after forming process are shown in Fig. 3. Before the forming process, resistance of the device stays in LRS in between –1.5V and 2 V. After the forming process with a single pulse of 3.5 V/ 80 ns, the bipolar resistive switching can be observed under the same sweeping voltage range and the RESET resistance is 12 k ohm, even after a RESET pulse as low as 2V.

In Fig. 4, the sweeping voltage is increased to 3V. Before forming, a shallow RESET/SET resistance window between 5 k ohm and 1 k ohm can be established by bipolar operation between 3V and –1.5V. After the forming process, the RESET resistance increases to nearly 2.5 times. It is notable that the LRSs before and after forming are almost the same but the HRSs are quite different. The forming process uses a pulse voltage higher than the RESET, and may terminate the unnecessary leakage paths in the high resistance state. The forming voltage as a function of via size is shown in Fig. 5. The forming voltage decreases as the via size scales down. This result implies the possibility for further scaling.

Figures 6 and 7 show the cycling endurances for the non-forming and forming devices, respectively. The non-forming devices develop severe resistance degradation after several tens of cycles. Because the non-forming device needs large RESET voltage (3.4 V) to reach the HRS, it is believed that the electrical stress due to the high RESET voltage results in the resistance degradation. A significant improvement in RESET-state distribution is observed after the forming device. The RESET state is more stable and the RESET/SET resistive ratio is larger than 10. The insets of Figs. 6 and 7 illustrate the resistance distribution of the two states. Both devices show the distributions in HRS are wider than those in LRS. The wide HRS distribution may be due to the different amount of leakage path remaining in the WO_x film during the switching cycles. These results reveal the forming process efficiently improves the switching stability of WO_x RRAM.

Figures 8 and 9 show the read-disturb tests on RESET and SET states, respectively. Severe read disturbance of RESET state is found for the non-forming device even after reading at 0.25 V for less than 100 sec. The read operation for RESET and SET states requires only 0.25 V, and the forming device is excellently immune to the read disturb below 0.4 V. The cases all show poor results at 0.8 V. These results are reasonable because the voltage almost reach to the resistive-switching voltage from LRS to HRS.

4. Conclusions

An electrical forming process based on a single voltage pulse has been demonstrated. The forming process has the advantage of low-voltage and fast-speed operation. This new forming process efficiently minimizes the RESET/SET dispersion and further improves the switching stability of WO_x RRAM.

References

[1] Y. H. You *et al*., Appl. Phys. Lett. **89** (2006) 222105.
[2] C. Yoshida *et al*., Appl. Phys. Lett. **91** (2007) 223510.
[3] H. B. Lv *et al*., IEEE Electron Device Lett. **29** (2008) 47.
[4] C. Y. Lin *et al*., IEEE Electron Device Lett. **28** (2008) 366.
[5] C. Y. Lin *et al*., J. Electrochem. Soc. **154** (2007) 189.
[6] I. G. Baek *et al*., *IEDM, Tech. Dig*. (2004) 587.
[7] C. H. Ho *et al*., *VLSI Tech. Dig.* (2007) 228.

Table I Comparison of the forming process parameters of different metal oxides

Oxide	Mode	Switching	Voltage	Speed
WO_x	**Pulse**	**LRS→HRS**	**3.5 V**	**80 ns**
NiO_x[1]	DC	HRS→LRS	8.1 V	>>80 ns
TiO_2[2]	DC	HRS→LRS	5 V	>>80 ns
CuO_x[3]	DC	HRS→LRS	16.5 V	>>80 ns
ZrO_2[4]	DC	HRS→LRS	8.8 V	>>80 ns
Al_2O_3[5]	DC	HRS→LRS	11 V	>>80 ns

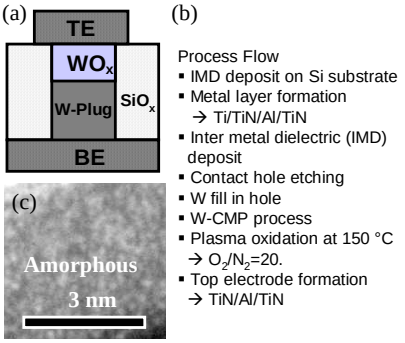

Fig. 1 (a) A cartoon of the cell structure, (b) process flow for fabricating the device, and (c) TEM image of the WO_x layer.

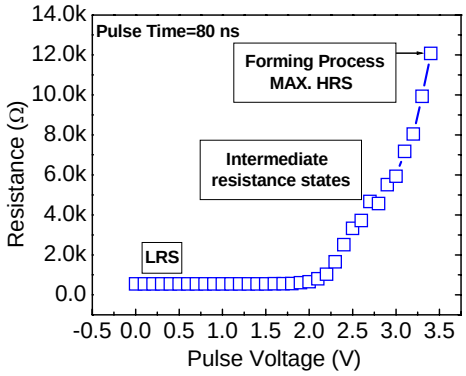

Fig. 2 Device resistance dependence on the pulse voltage. The device resistances increases gradually from LRS to HRS. Read voltage for each point is 0.25 V.

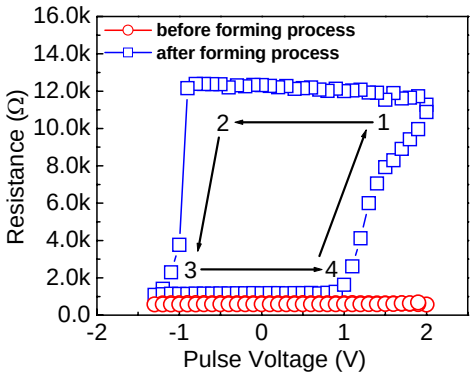

Fig. 3 Hysteresis loops of the device before and after forming process. The programming pulse of 80 ns decreases from 2 V to –1.5 V and then increase back to 2V for each loop. The resistance is measured at 0.25 V after each programming pulse. After the forming process, the device performs the bipolar resistive switching.

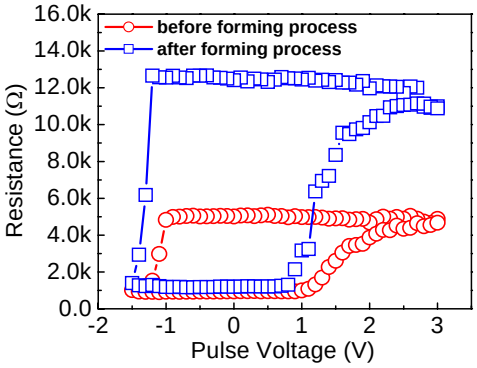

Fig. 4 Hysteresis loops between 3 V and –1.5 V. Before forming, the maximum resistance is 5 k ohm. After forming process, the resistance window opens up to 2.5 times of that before forming.

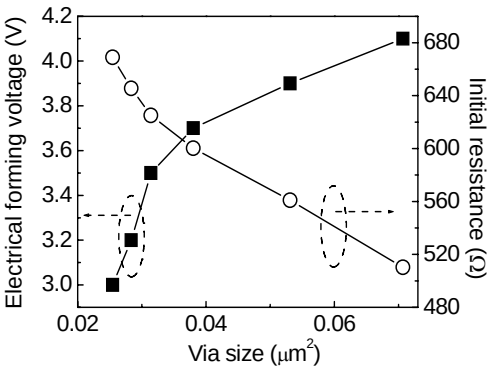

Fig. 5 Forming voltage and initial resistance as a function of cell size.

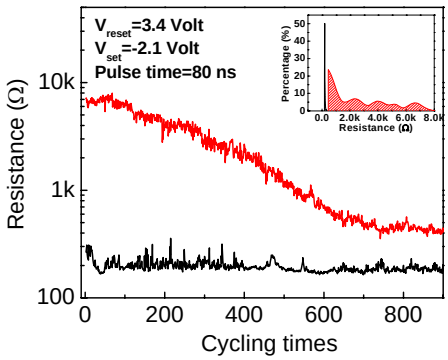

Fig. 6 Cycling result of the device without forming. The inset figure shows the R_{reset} and R_{set} distributions.

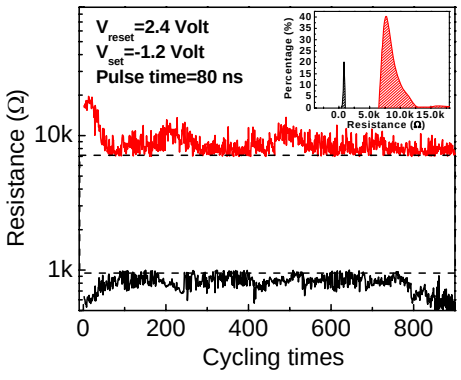

Fig. 7 Cycling result of the device with forming. The inset figure shows the R_{reset} and R_{set} distributions.

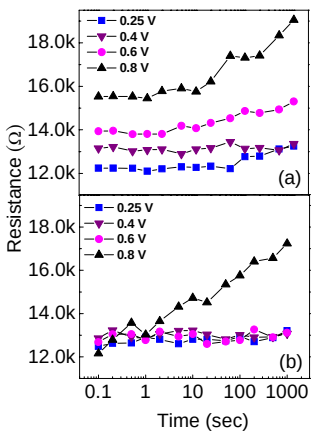

Fig. 8 Read disturb test on RESET states for (a) non-forming and (b) forming devices. No read disturb is observed below 0.6 V for the device with forming process.

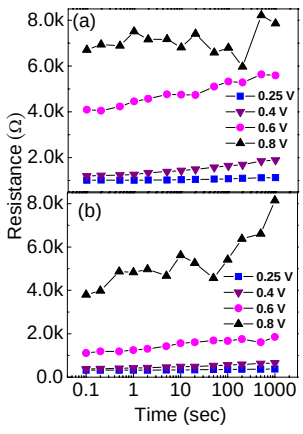

Fig. 9 Read disturb test on SET states for (a) non-forming and (b) forming devices.