

Multi-Level Switching Characteristics for WO_x Resistive RAM (RRAM)

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1. Introduction

Recently, resistance-based memory has attracted much attention for high-density memory applications because of its simple structure, small cell size, high speed, low power consumption, and potential for 3D stacking [1-2]. Tungsten oxide (WO_x) is an electrochromic material that reversibly changes optical properties in response to pulse voltage. This property is employed in optical devices such as smart windows for transmittance modulation [3]. In our previous works, we demonstrated that WO_x is not only suitable for optical devices but also for resistance-switching devices [4-5]. Though multi-level storage is an efficient way to increase the data density and reduce the process cost, few reports demonstrate the multi-level switching of the transition metal oxide (TMO) RRAM and the cycling number is still poor [6]. In this paper, we investigate the multi-level switching behavior of graded WO_x structure for high-density nonvolatile memory application. The conducting behaviors of the devices are also addressed.

2. Device Fabrication

Fig. 1 shows the cell structure and cross sectional TEM image of the graded WO_x based resistance memory. The fabrication process flow follows the conventional back-end-of-line W-plug process and the active area is located between the W bottom electrode (BE) and the TiN top electrode (TE). The diameter of the W-plug is 0.17μm. The graded WO_x between the tungsten plug and the top TiN electrode was prepared by down stream plasma oxidation (400 sec) in a mixture of nitrogen and oxygen at 150°C.

3. Results and Discussions

Fig. 2 shows the DC IV sweep switching of WO_x. From step A to B is the RESET process. An increase of voltage results in a metal like increase in current in step A, followed by an abrupt drop of the current between 1V and 1.3V in step B. After RESET to high resistance, the SET process occurs from step C to D at higher voltages. The current suddenly increases and rapidly reaches the current compliance limit, 7mA. The above DC experiment indicates the low operation voltage for WO_x based RRAM. In a conventional TMO RRAM device, the RESET to SET or SET to RESET transition are both very steep. As a result, there is no practical room for multi-level operation and only several cycle times have been demonstrated [6]. To evaluate the possibility of multi-level operation of the WO_x

device, the resistance as a function of pulse voltage is measured, with square pulses of 50 ns, as shown in Fig. 3. The resistance gradually increases from low resistance state (LRS) to high resistance state (HRS) as the voltage increases until 3.1V, an indicative for high probability of multi-level switching. For bipolar switching of WO_x RRAM, negative pulses are used to SET the device, and positive pulses are used to RESET the device [4]. We also use the same method to obtain the multi-level switching. The state 00 is the LRS obtained by using SET process of -2V and 100ns. The HRS states 01, 10, and 11 are obtained by applying 50ns of 2.5V, 2.7V, and 3V pulses, respectively. As shown in Fig.4, the operation sequence of the multi-level cycling follows the state 00 → 01 → 10 → 11 and back to 00 (Method A). The resistance window between each state is nearly 2k ohm, and memory windows are maintained after cycling 100 times. A closer inspection of the four states shows that while state 00 is well controlled, the resistances at HRS states fluctuate from cycle to cycle. To eliminate this HRS fluctuation a new operation sequence is adopted, in which the device is always SET to the 00 state before programming to HRS states 01, 10 and 11 (Method B). The 00 LRS state is still well controlled while the HRS states are more predictable as shown in Fig. 5. Fig. 6 shows the standard deviation (σ) and average resistance ($\bar{R}$) of the states 00 to 11 by using method A and B, respectively. The 11 HRS state for Method B is significantly reduced. Fig. 7 shows the IV characteristics of the states 00 to 11. The slopes in the low electric field region from 0.01V to 0.2V for all four states are very close to 1; this indicates Ohmic conduction. In the medium electric field region (from 0.2V to 0.6V), the current is proportional to the square of the applied voltage. This implies that the space charge limited current (SCLC) is dominating the conducting behavior in this range ($J = 8\epsilon u V^2 / 9d^3$). Above 0.6V, the resistance states change to HRS until the voltage reaches 1V, similar to the DC behavior shown in Fig. 2. When voltages decrease from 1V to 0.01V, all states show the same trend of IV characteristics of HRS. Therefore, it shows the hysteresis behavior of the states 00, 01, and 10, and no hysteresis of the state 11 because it is HRS already and doesn't change anymore by applied voltage to 1V. Fig. 8 shows the read disturb behavior of applied voltage between 0.2V to 0.6V for all states. The states 10, and 11 show essentially no

disturb and the states 00, and 01 show good immunity to read disturb up to 0.4V.

4. Summary

By varying the programming voltage pulses, the resistance of WO_x based RRAM devices can be well controlled and we have demonstrated multi-level switching characteristics of the devices. The fluctuation and DC conducting behavior of different resistance levels are analyzed, and reliability tests show far better performance than previously reported.

References

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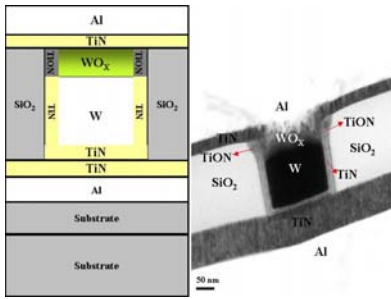


Fig. 1. Cell structure and cross sectional TEM image of the WO_x RRAM

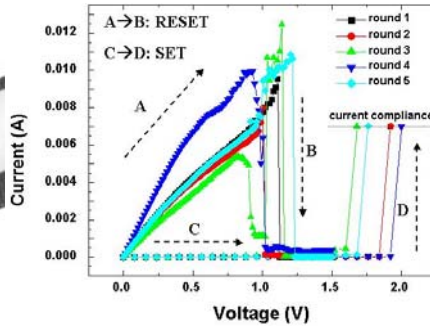


Fig. 2. The RESET, and SET processes of WO_x RRAM by DC IV sweep.

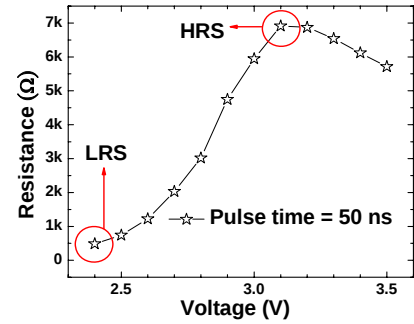


Fig. 3. The resistance dependence of the applied voltage with fixed pulse time 50 ns.

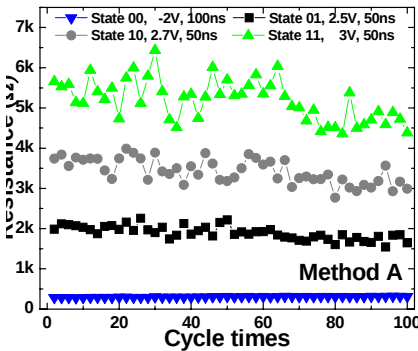


Fig. 4. 4-level cycle operation of the WO_x RRAM (Method A). 3 levels are RESET status with different positive pulses and 1 level is SET status with a negative pulse.

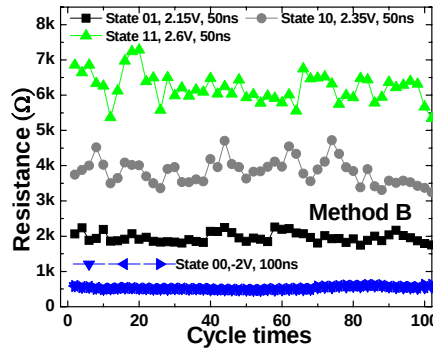


Fig. 5. Another operation sequence method by using erase state 00 first before forming HRS states 01, 10, and 11 (Method B).

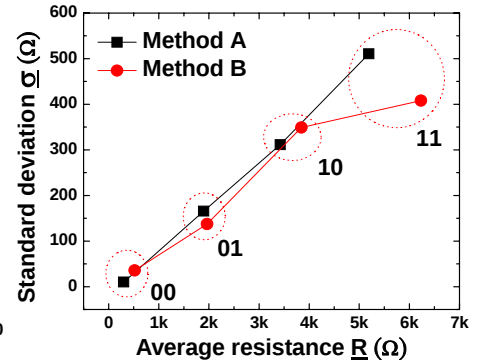


Fig. 6. The standard deviation versus the average resistance by using method A and B, respectively.

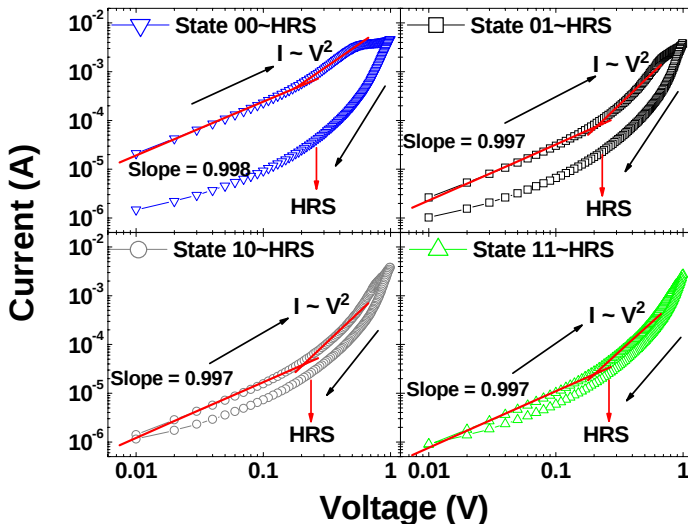


Fig. 7. IV curves and their fitting results. I-V curves obey ohmic conduction in the low voltage region, but show SCLC behavior in the high electrical field region.

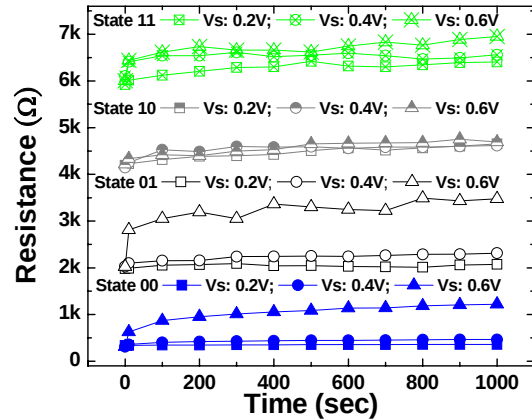


Fig. 8. Read disturb test on WO_x device. The states 10, and 11 is not affected by the read bias of 0.2 to 0.6V. The states 00, and 01 are immune to read disturb under bias below 0.4V.