Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 354-355

P-1-11

Electrical Stress-Induced Degradation of HfAlO and HfO_2 Films of Equal EOT

Piyas Samanta[1,2], Yao-Jen Lee[3], Chin-Lung Cheng[4] and Mansun Chan[2]

[1]Physics Department, Vidyasagar College for Women, 39 Sankar Ghosh Lane, Kolkata 700 006, India
[2]Department of Electronic and Computer Engineering, Hong Kong Univ. of Sci. and Tech., Kowloon, Hong Kong SAR
[3]National Nano Device Laboratories, Hsinchu, 30078, Taiwan
[4]Institute of Mechanical and Electro-Mechanical Engineering, National Formosa University, Huwei, Yunlin, 63201, Taiwan

1. Introduction

Among various hafnium based oxides viz. hafnium oxide (HfO_2) [1,2] and its alloy with Al_2O_3 [3,4], hafnium aluminate (HfAlO) has become attractive for the next generation gate dielectric material because of its various superior qualities. In past few years, a considerable progress has been achieved in understanding the electrical and material properties of HfAlO films [3–6]. However, no consensus has been reached in charge carrier trapping related oxide deterioration in HfAlO and HfO_2 films. Therefore, we attempt to investigate the charge carrier generation/trapping in both HfAlO/SiO_2 and HfO_2/SiO_2 layered dielectrics of equal equivalent oxide thickness (EOT) and compare the related oxide degradation and device performances during constant voltage stress (CVS).

2. Experimental

Devices used here were nMOS capacitors with TaN gate on HfAlO (2.0 nm)/SiO_2 (2.0 nm) and HfO_2 (3.8 nm)/SiO_2 (2.0 nm) layered dielectrics on (100) oriented boron doped silicon wafers of 15–25 and 4–8 Ω cm resistivities, respectively. The HfAlO films were deposited from a HfO_2–Al_2O_3 combination with 1:1 weight ratio. The HfO_2 films were deposited by Jusung MOCVD process. Both wafers were received backside aluminum deposition for Ohmic contact and for minimizing series resistance effects. DC stress and sensing measurements were done at room temperature in a dark shielded chamber on several identical test structures. The estimated EOTs from full quantum mechanical (QM) simulation of the measured 100 kHz *C*–*V* results were 2.63 nm in both stacks.

3. Results and Discussions

Fig. 1 shows larger hysteresis in as-fabricated HfAlO samples compared to virgin HfO_2 devices of equal EOT indicating existence of larger amount of border trap [2] in the former devices. Time evolution of tunnel current density J_g during CVS depicted in Fig. 2 indicates the absence of electron trapping in the HfAlO/SiO_2 stack contrary to the HfO_2/SiO_2 stack. The non-saturating behavior of J_g in both devices indicate neutral trap creation in the bulk. However, in both samples, positive charge trapping close to the Si/SiO_2 interface was observed as evident from the negative shift of the high-frequency *C*–*V* curves after CVS relative to the fresh devices shown in Fig. 3. Stress-induced oxide positive charges ΔN_{ot}^{+} were quantified using the estimated midgap voltage shift (ΔV_{mg}) relative to the fresh device [2]. A relative comparison of oxide positive charge trapping rate in both devices is shown in Fig. 4. The enhancement of ΔN_{ot}^{+} in HfAlO stack is possibly due to larger concentration of non-bridging oxygen centers originated from breaking of Al–O–Al bonds. Since memory application is related to oxide charge trapping, larger value of ΔN_{ot}^{+} at a given voltage indicates better performance of HfAlO devices in memory applications when compared with HfO_2/SiO_2 stack of same EOT. Both devices exhibit interface state generation during CVS. From the single 100 kHz frequency *C*–*V* and *G*–*V* plots [7], density of stress-induced surface states ΔN_{it} were estimated and the results are shown in Fig. 5. Addition of Al increases the Si/SiO_2 interface stability in devices both before and after CVS (Fig. 5). Therefore, we propose that stress-induced channel carrier mobility and transconductance degradation in MOSFETs with HfAlO gate dielectric is lower than that with HfO_2 of equal EOT. It is interesting to note that both ΔN_{ot}^{+} and ΔN_{it} follow $t^{0.2}$ power-law in either of the samples indicating the similar generation kinetics for these two type of defects [2]. The threshold voltage degradation ΔV_T is a cumulative effect of stress-induced ΔN_{ot}^{+} and ΔN_{it}. However, comparing the results shown in Figs. 4–6, we argue that ΔN_{ot}^{+} contributes more in ΔV_T degradation. Similar to ΔV_T degradation, SILC degradation and hence the neutral trap creation rate is higher in HfAlO devices compared with HfO_2 samples of equal EOT as illustrated in Fig. 7. The results shown in Figs. 6 and 7 immediately imply that the dielectric breakdown triggered by neutral trap creation and/or bulk positive charge trapping is facilitated in HfAlO samples relative to HfO_2/SiO_2 stack of equal EOT.

4. Conclusions

We have presented a detailed investigation on relative comparison of electrical stress-induced gate dielectric degradation and device performances with HfAlO and HfO_2 films of same EOT. Our results indicate that HfAlO samples are superior to HfO_2 samples in memory and CMOS logic applications. On the other hand, compared to the HfO_2 devices, the HfAlO samples exhibit a higher rate of oxide charge trapping and neutral trap creation at a given stress voltage. These in turn results V_T and SILC degradations higher in HfAlO devices. In other words, at a given operating voltage, the device life time is shorter in HfAlO samples relative to HfO_2 samples of equal EOT. Furthermore, both oxide bulk and interface trap creation follow the same generation kinetics possibly due to dispersive proton transport [2].

Acknowledgement

P. Samanta would like to thank Dr. S. Mahapatra at Microelectronics Division, IIT Bombay for financial support and providing the measurement facilities.

References

[1] G. D. Wilk, R. M. Wallace and J. M. Anthony, J. Appl. Phys. **87** (2000) 484.

[2] P. Samanta, C. Zhu and M. Chan, Microelec. Engg. **84** (2007) 1964.

[3] W. Zhu, T. Tamagawa, M. Gibson, T. Furukawa and T. P. Ma, IEEE Electron Device Lett. **23** (2002) 649.

[4] S. H. Bae, C. H. Lee, R. Clark and D. L. Kwong, IEEE Electron Device Lett. **24** (2003) 556.

[5] V. Mikhelashvili, B. Meyler, J. Shneider, O. Kreinin and G. Eisenstein, Microelec. Reliab. **43** (2005) 933.

[6] W. Loh, B. J. Cho, M. S. Joo, M. F. Li, D. S. Chan, S. Mathew and D. L. Kwong, IEEE Trans. Dev. and Mat. Rel. **4** (2004) 696.

[7] W. A. Hill and C. C. Coleman, Solid-State Electron. **23** (1980) 987.

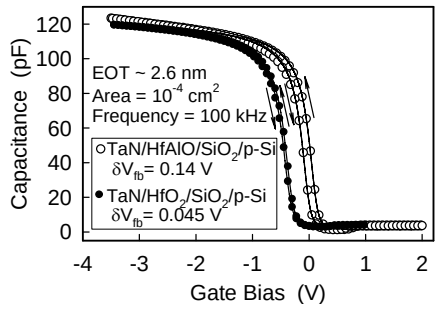

Fig. 1 Bi-directional *C–V* plot in fresh devices with $HfAlO/SiO_2$ (open) and HfO_2/SiO_2 (solid) stacks. Curves are from QM simulation.

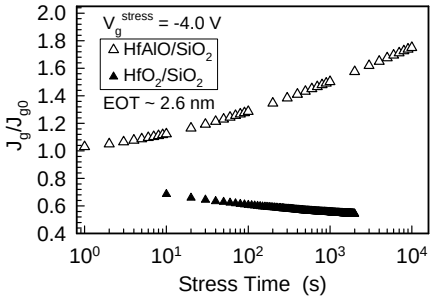

Fig. 2 Tunneling current density normalized to its initial value as a function of stress time during CVS at –4.0 V.

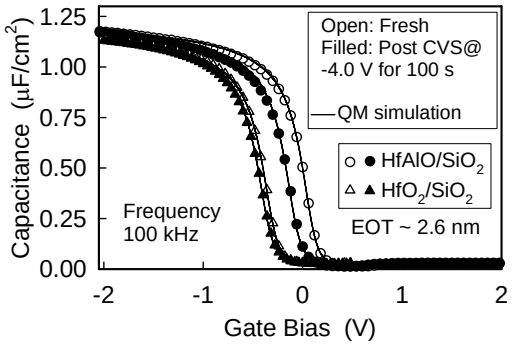

Fig. 3 High-frequency *C-V* curves recorded before and after CVS at –4.0 V for 100 s with $HfAlO/SiO_2$ (circle) and HfO_2/SiO_2 (triangle) stacks.

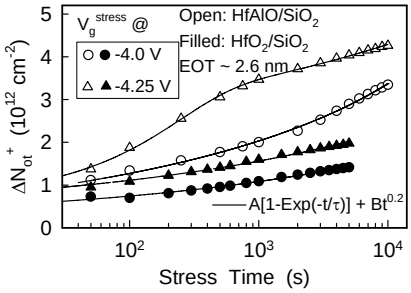

Fig. 4 Area density of oxide trapped charges as a function of stress time in $HfAlO/SiO_2$ (open) and HfO_2/SiO_2 (solid) stacks with stress voltage as a parameter.

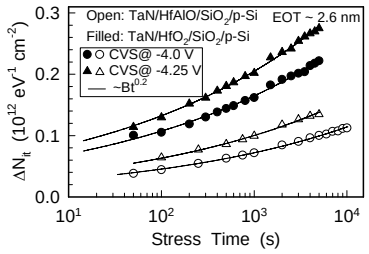

Fig. 5 Area density of stress-induced interface states as a function of stress time in $HfAlO/SiO_2$ (open) and HfO_2/SiO_2 (solid) stacks with stress voltage as a parameter.

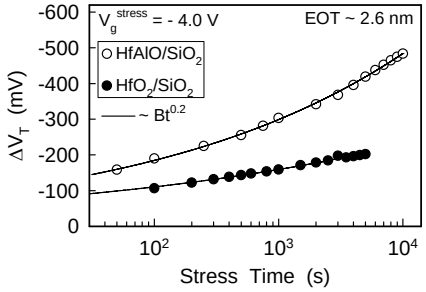

Fig. 6 Threshold voltage shift relative to the fresh device as a function of stress time in $HfAlO/SiO_2$ (open) and HfO_2/SiO_2 (solid) stacks during CVS at –4.0 V.

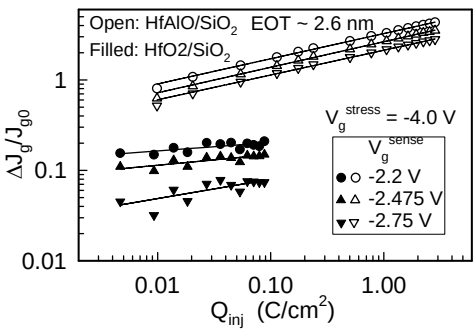

Fig. 7 Normalized SILC as a function of injected electron fluence in $HfAlO/SiO_2$ (open) and HfO_2/SiO_2 (solid) stacks after CVS at –4.0 V with sensing voltage as a parameter.