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Trap-Related Carrier Transports in p-FET with Poly-Si/HfSiON Gate Stack

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1. Introduction

It is expected that Hf-based high-k gate dielectrics will replace silicon dioxide in the near future. However, it is necessary to have a better understanding of the leakage and breakdown physics of high-k devices before putting into production. Our recent studies have clarified that there is a significant difference between the leakage behaviors of p- and nMOS with poly-Si/HfSiON gate stack as revealed by electron-beam-induced current (EBIC) technique. [1] In pMOS with p^+poly-Si gate electrode, there may exist high-density charged traps, which act as tunneling paths for holes. [2] We are interested in the trap-related carrier transports through high-k dielectrics. In this study, we performed EBIC observations under different injection conditions, including electron injection from gate, hole injection from substrate, and co-injection of electrons and holes. Thus, it is possible to investigate the transportation processes of electrons and holes under individual or combined injections.

2. Experimental

The devices used in this study were p-FET with p^+poly-Si/HfSiON gate stacks. The size of gate region was 20×20 μm^2. The physical thickness of HfSiON was 3.5 nm. Between HfSiON layer and Si substrate, there is a SiO_2 interfacial layer with a thickness of 0.7 nm. Above HfSiON, there existes gate electrode consisted of p^+poly-Si (105 nm) and NiSi (22 nm). The whole MOSFET is capped with a thick SiO_2 (300 nm) layer for surface isolation.

For EBIC measurement, the electrodes of gate and substrate were connected to a current amplifier. A bias voltage was applied to the gate electrode. The electron-hole pairs generated by electron beam are separated and collected by an electric field to form a current signal. In this study, the accelerating voltage of electron-beam (V_{acc}) and gate bias voltage (V_G) are two important parameters for realizing the carrier separation. The generation volume of e-h pairs in a material is mainly determined by the V_{acc}. The electron range is used to characterize the dimension of this generation volume, namely the penetration depth of electron beam. In this study, the V_{acc} varied from 5 to 12 kV, which corresponded to an electron range from 300 to 1200 nm. Thus, by choosing proper V_{acc}, it is able to control the generation of carriers in Si substrate or not. On the other hand, by applying proper bias voltage, it is able to change the carrier injection condition according to the band alignment and band bending of MOS structure.

3. Results and Discussion

Figure 1 shows typical EBIC images of the gate regions of p- and n-FETs. The images were taken at 9 kV under depletion bias voltages (-0.5 V for p-FET and 0.5 V for n-FET). In the p-FETs, the gate region appeared as a dark background with lots of bright spots inside. These bright spots are the sites with enhanced current. While in the n-FET, the gate region appeared as a bright background with a rather uniform background current. The background current of n-FET is one or two orders higher than that of p-FET. We have discussed in our previous work that the bright spots were related to the trap-assisted tunneling path of holes in HfSiON layer. [2]

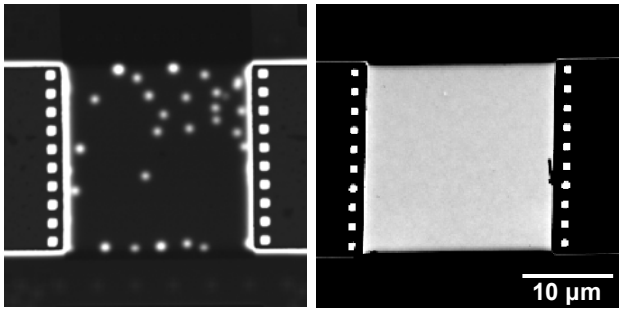

Fig. 1 Typical EBIC images of p- and n-FETs.

In the following, we will focus on the EBIC results of p-FET. Figure 2 shows three EBIC images of a p-FET taken under three injection conditions, namely hole injection, electron injection, and co-injection of both carriers. Correspondingly, the schematic carrier transport processes under these injection conditions were also illustrated Fig. 2.

To realize hole injection, it is supposed that the V_{acc} is large enough to reach to the Si substrate, and the V_G should be small enough to prevent the electron injection from gate electrode (such as $V_{acc} > 5$ kV, $V_G = 0$ V). The EBIC image

shows lots of bright spots appeared in the gate region with a dark background (current below detection limit). The current is dominated by hole injection from Si substrate, and the conduction mechanism of holes is trap-assisted tunneling.

To realize electron injection, it is supposed that the V_{acc} should be small not to generate carriers in the Si substrate, and the V_G is large enough to lead to the electron injection from gate electrode (such as $V_{acc} \leq 5$ kV, $V_G = -2$ V). There is a strong background current (~ 400 nA) passing through high-k. However, no specific defects are detected in the gate region. The current is dominated by the electron injection from gate electrode, and the conduction of electron is independent of defects in high-k.

For the co-injection condition, both V_{acc} and V_G were kept large enough to realize the co-injection of hole and electron (such as $V_{acc} > 5$ kV, $V_G = -2$ V). The EBIC image shows lots of dark spots (with decreased current) appeared in the gate region with a strong background current. It should be noted that the local distribution of dark spots in Fig 2(c) is almost as same as that of bright spots in hole injection condition (Fig 2(a)). The current is contributed by both carriers, and a recombination-like process may take place at the defect positions. Otherwise, it is speculated that the such defects act as the tunneling paths for hole conduction but blocking sites for electron conduction at the same time. The maximum contrast of both bright and dark spots appeared at 8 kV, suggesting that the more enhanced hole transport the more suppressed electron transport.

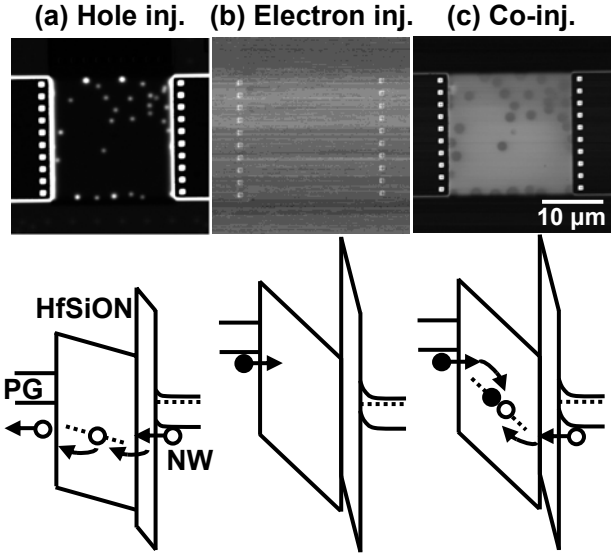

Fig. 2 EBIC images (up) and schematic carrier transport processes (bottom) of pMOS under three injection conditions.
(a) Trap assisted hole tunneling from substrate;
(b) Independent electron-injection from gate;
(c) Co-injection of electron and hole, recombination occurs.

4. Conclusions

The trap-related transport mechanisms of electron and hole through high-k p-FET were clarified by performing EBIC measurements under different carrier injection conditions. On the condition of individual hole or electron injection, the conduction of hole is strongly enhanced by trap-assisted tunneling, while the conduction of electron is independent of traps. On the condition of co-injection of electron and hole, trap-assisted hole conduction and electron trapping may occur together, leading to a recombination-like process.

References

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[2] J. Chen, T. Sekiguchi, N. Fukata, M. Takase, T. Chikyo, K. Yamabe, R. Hasunuma, M. Sato, Y. Nara, and K. Yamada, IEEE IRPS proc. (2008) 584.