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Significance of Interface Layer between Surface Layer and Si Substrate in Plasma-Exposed Structures and Its Impacts on Plasma-Induced Damage Analysis

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1. Introduction

Plasma processing has become essential in the micro-electronic industries to fabricate finer patterns. As feature size of devices has shrunk, plasma-induced damages (PID) can no longer be neglected. Ion-bombardment damage, one of the PID mechanisms, is realized as "Si recess" [1] (Fig. 1). The size of the recess is to be in conflict with device design margin, and controlling layer thickness will be crucial in scaled devices [2]. We have identified by a photoreflectance spectroscopy (PRS)–based technique that plasma-exposed surface region includes latent defects of significant order ($>10^{12}$ cm^{-2}), in particular, near the interface between surface and Si substrate [2, 3]. However, there have been few detailed studies of plasma-damaged surface structures which play important roles in device characteristics. In this study, we analyze in detail the structure of plasma-exposed Si surface by focusing on the interface layer (IL) structure. We employed spectroscopic ellipsometry (SE) [4], PRS [2, 3], transmission electron microscopy (TEM), molecular dynamics (MD) simulation, Rutherford backscattering spectroscopy (RBS) and capacitance-voltage (C-V) measurement to investigate the structures. Based on comprehensive analyses, we provide a key issue, *e.g.,* that conventional methodology can lead to an erroneous conclusion in addressing the structures and clarifying the PID mechanisms.

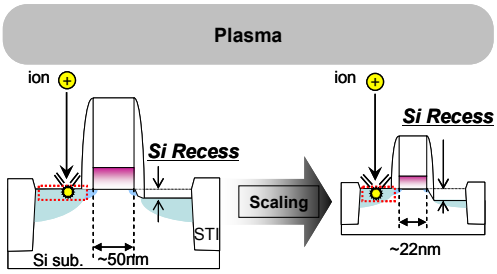

Fig. 1 Schematic illustration of substrate damage by energetic ion bombardment usually associated with "Si recess". Although the feature size of MOSFETs has shrunk dramatically, thickness of Si recess is believed to be unchanged and will be in conflict with device size such as source/drain extension depth in the near future.

2. Experimental

N-type (100) silicon wafers (0.02 Ωm) were mounted on an ICP (inductively coupled plasma) chamber stage. Ar gas was utilized in order to eliminate chemical reactions. Chamber pressure was 20 mTorr. The wafers were exposed to the plasma for 30 seconds. Source power (responsible for determining plasma density and electron temperature) was 300 W. 13.56 MHz bias with the power ranging from 0 W (no bias) to 400 W was applied to control ion energies. The waveform of the bias was monitored near the stage by an oscilloscope, and a self-bias voltage (V_{dc}) was measured. Since plasma potential was ranging from 11 to 16 V in these configurations, V_{dc} approximately corresponds to the mean ion impact energy to the surface [5].

Two optical analyses, SE and PRS, were conducted to identify damaged layer thickness and defect density. In SE analysis, data was fitted against two optical models: model A is a commonly and widely used three-layer model (ambient/SiO_2/substrate) and model B is a four-layer model (ambient/SiO_2/interface/substrate). Interface layer (IL) was modeled as a composite of SiO_2 and crystalline Si with Bruggeman's effective medium approximation (EMA). Parameters were determined by minimizing mean square deviation (δ). Also the defect density in IL was analyzed by the PRS-based model for comparison [2, 3]. TEM, MD simulation, RBS and C-V measurement were carried out to clarify the structure.

3. Results and Discussion

Table I shows the results of SE using models A and B. Increase in thickness can be observed with model A for higher bias powers. Large δ at > 200 W indicate deviation from model A. Meanwhile, using model B, we obtained smaller δ (better fit) for each configuration. As V_{dc} increased, the surface layer (SL) thickness (d_1) decreased and IL (d_2) became predominant at around $|V_{dc}|>200$ V (Fig. 2). From this figure we can see that the total layer thickness (d_1+d_2) saturates at 5 nm. The PRS-based analysis also estimates (not shown) the defect density in the vicinity of IL ranging from 6.9×10^{12} to 2.0×10^{13} cm^{-2} with an increase in V_{dc} in the present study.

Table I. Results of SE analysis for Si wafers processed with Ar plasma at 20 mTorr. Rf bias power was varied as shown.

	Bias (W)	V_{dc} (V)	Model A		Model B			
			d (nm)	δ	d_1 (nm)	d_2 (nm)	f_{Si} (%)	δ
A	0	-	2.6	0.0090	2.1	0.3	29.2	0.0083
B	25	-33	4.2	0.0112	3.8	0.4	22.2	0.0109
C	50	-82	5.0	0.0155	3.7	1.0	27.2	0.0128
D	75	-115	5.6	0.0200	3.5	1.4	32.4	0.0122
E	100	-130	5.1	0.0187	3.4	1.2	29.0	0.0141
F	150	-161	5.1	0.0243	2.4	1.9	23.5	0.0156
G	200	-200	5.2	0.0286	2.3	2.1	23.0	0.0206
H	250	-246	5.8	0.0344	1.7	2.9	23.3	0.0201
I	300	-282	6.3	0.0400	1.2	3.7	25.5	0.0140
J	400	-400	4.4	0.0609	0.0	3.2	30.0	0.0420
Control		-	1.3	0.0091	1.3	0.0	-	0.0091

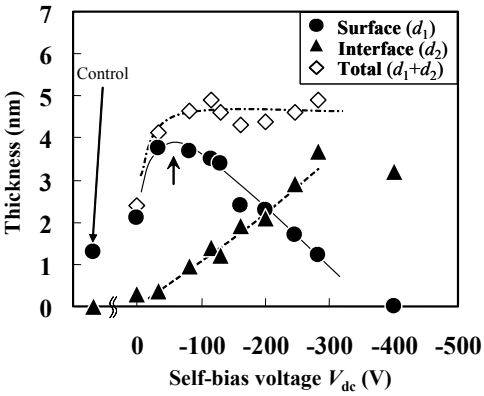

Fig. 2 Thickness of surface layer (d_1) and interface layer (d_2) obtained by four-layer model B. Total damage layer thickness (d_1+d_2) is also shown. Results for samples processed without bias is plotted as $V_{dc} = 0$. The lines are to guide the reader's eye.

Fig. 3(a) shows a TEM image of a sample which corresponds to process E in Table I. Layer thickness was found to be 4.6 nm. We have compared this with the SE results in Fig. 3(b). Model B showed better agreement with TEM. Closer observation of the interfacial region reveals that crystalline orientation is preserved for several monolayers towards the surface. This is in good agreement with model B not only in terms of IL thickness (as illustrated in Fig. 3(b)), but also meets the assumptions of EMA.

Previous MD simulation studies showed that typical sputtering thresholds for Ar impacting Si and SiO_2 targets are at around 50 eV [6]. Thus, the decrease in d_1 assigned in Fig. 2 (indicated by an arrow) is considered to be attributed to physical sputtering of the surface. When ions (Ar and/or O) bombard the surface, they may scatter oxygen atoms present in the native oxides and penetrate into the substrate. The phenomenon intensifies with higher ion energies, *i.e.* higher V_{dc}. The resulting layer would be partially oxidized, and would be recognized by SE as the IL. In order to confirm these mechanisms, we have further developed a MD simulation using Stillinger–Weber type interatomic potentials [7]. One of the results is shown in Fig. 4(a). The results were comparable with TEM and SE. A previous study [4] proposed a model consisting of SiO_2 and amorphous Si as SL. However, the results obtained here by SE,

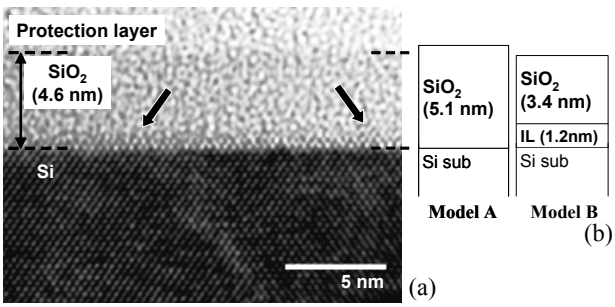

Fig. 3 (a) A [110] cross-sectional TEM micrograph of a Si (100) wafer exposed to Ar plasma under 100 W rf bias. While most of the oxide layer is non-crystalline, some regions near the interface retain the crystalline orientation of the substrate in the direction indicated by arrows. (b) SE measurements for the same configuration are compared to scale. Note that IL corresponds to the region where crystalline structure is observed by TEM. Model A results in thicker SL.

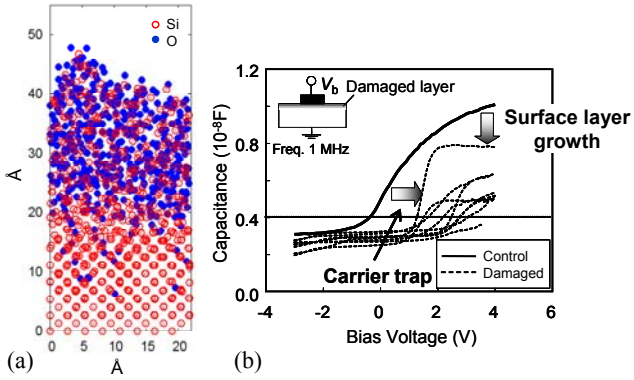

Fig. 4 (a) A snapshot of a MD simulation for a wafer processed with Ar plasma discussed in this study. Ar beam is directed into the surface at 130 eV, at normal incident angle. (b) Capacitance-voltage curves obtained by mercury probe system. Surface layer growth lowers capacitance at positive voltages. Carrier traps are discussed elsewhere [8].

TEM and MD identified the SL as stoichiometric SiO_2, which is also supported by RBS (not shown here). Furthermore, the structure observed by above techniques was also confirmed as distortion of the capacitance-voltage (C-V) curve as shown in Fig. 4(b).

4. Conclusion

We have analyzed the ion-bombardment damage by an ICP system from viewpoints of optical analyses, MD simulation and C-V characteristics. We have confirmed that an appropriate and accurate model for plasma-damaged silicon surface structures should include an interface layer between the surface layer and the substrate. This was supported by both MD simulation and C-V measurement. We have also assigned surface sputtering and more severe damage at high bias voltages, resulting in larger defect densities in IL. Note that the defects in IL assigned here will remain even after a wet etch process and degrade device performance. The results in this study indicate that conventional models may yield inaccurate damage analysis, and that consideration of an interface layer is inevitable for precise damage control.

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