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Thermal Stability of High-κ Dielectrics – A Nanocharacterization Perspective

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1. Introduction

Thermal stability is one of the major selection criteria for the next generation high-κ gate dielectric [1]. At high temperature, silicidation can happen at the high-κ/Si interface, resulting in an additional silicide layer that shorts out the field effect. The effect of post deposition annealing (PDA) to Lanthana has been examined by *CV* [2] and localized *IV* [3]. In this study, we show that both low and high temperature PDA increase non-uniformity of the gate stack, but due to different mechanisms. The optimum annealing temperature occurs at an intermediate range (~500ºC). However, traps are still generated readily in the 500ºC annealed film under electrical stress. The generated electronic traps are observed to be uncorrelated to the defects that are responsible for the *CV* hysteresis.

2. Experimental

The bi-layer gate stack, consisting of 3 nm Sc_2O_3 (top) and 4 nm La_2O_3 on a n-Si substrate, was prepared by electron-beam vapor deposition in ultra-high vacuum (UHV). PDA was done in nitrogen at different temperatures. STM was carried out using a W tip in Constant Current Imaging (CCI) mode in UHV, with the bias (V_s) applied to the substrate. Spatially resolved *IV* was acquired simultaneously during CCI [Constant Current Tunneling Spectroscopy (CITS)]. CITS current maps sensitively reflect local potential barrier variation in the high-κ or SiO_x interfacial layer (IL) [4]. Leakage current is defined as current having a value 20% higher than the median of the current distribution within the scanned area (Fig. 1)

3. Results and Discussion

Effect of PDA on electrical uniformity in the high-κ gate stack

Fig. 2 shows the STM CCI image (I) and CITS current map at +2.3V (II) for (a) as-deposited, (b) 300ºC, (c) 500ºC and (d) 700ºC annealed samples. The sample bias for leakage current monitoring is chosen as +2.3V as leakage observed at this bias regime will be from tunneling through band gap states of the high-κ layer. Hence image (II) reflects the electrical quality of the high-κ film. The feedback set point for (I) (-4V, 20pA) provides data relatively independent of the high-κ property based on the polarity dependence of the STM current [4]. For better visualization of the electrical uniformity, the current distributions from (II) for the 4 samples are shown in the normalized cumulative plot in Fig. 3. The current is normalized to the median of the distribution for comparison of uniformity across different samples. The area of the sample having leakage current exceeding 20% of the median current is estimated as 33%, 46%, 32% and 39% for Fig. 2 (a) to (d), respectively. X-ray Photoelectron Spectroscopy (XPS) analysis (Fig. 4) was also undertaken.

Localized leakage current occupies 33% of the scanned area in the as-deposited sample and can be attributed to the presence of $La(OH)_3$, which is suggested by the shift of the La3d peak to a higher binding energy [Fig. 4 (a), solid square] from the theoretical La_2O_3 peak, which is located at 834.5eV (with the Si2p peak at 99.3eV as reference)[5]. Low temperature PDA (300ºC) increases the non-uniformity of the gate stack and the leakage current occupies 46% of the scanned area. The increase in leakage as observed in STM could have the same origin as the positive charge induced by low temperature annealing observed from *CV* measurement [2]. XPS suggests partially absorbed La_2O_3 and $La(OH)_3$ exist in the film. Both phases are known to have a high density of positive charge, which may be the source of the increased leakage current.

Intermixing between Sc_2O_3 and La_2O_3 occurs at an annealing temperature of 500ºC and above, as indicated by a shift of the Sc2p peak to lower binding energy for the 500ºC and 700ºC annealed samples [Fig. 4(b) open square and circle]. La_2O_3 and LaScO phases co-exist in the film. The phase separation could result in localized leakage current. It is because the structural defects, due to imperfect interface between different phases, can assist in current conduction. The 500ºC annealed sample has the best electrical uniformity among the four samples under study. Further increase in the annealing temperature degrades the uniformity. This may be caused by the back-diffusion of Si into the high-κ film, as supported by the shift of the La3d peak to higher binding energy [Fig. 4(a), open circle], and the observed Si depth profile from Time-Of-Flight Secondary Ion Mass Spectrometry (Fig. 5).

Electrical Stress Induced Evolution

The as-deposited and the 500ºC annealed sample are shown to have relatively good uniformity. Electrical stress was applied to both samples by continuous CITS scan of a given area. *IV* is taken at locations free of pre-existing electronic traps (i.e. dark shades in the CITS current map) to monitor degradation of the gate stack. Trap generation in the high-κ layer is reflected by an increase in tunneling current at positive V_s. Fig. 6 and 7 show the extracted *IV* from 6 consecutive CITS scans of the as-deposited and 500ºC annealed films, respectively. No increase of tunneling current can be observed for the as-deposited film whereas current at positive V_s increases upon consecutive stress for the 500ºC annealed film. Although the result suggest the as-deposited film has better reliability performance, the film suffers from serious hysteresis, as shown by the *CV* characteristic in Fig. 8. This observation also suggests that the nature of the defects responsible for *CV* hysteresis may be different from that of the stress induced traps.

3. Summary

This STM study shows that PDA increases non-uniformity of the high-κ gate stack if the temperature is not chosen appropriately. The optimum annealing temperature for uniformity and hysteresis at an intermediate temperature of around 500ºC. Electronic traps are generated readily in the 500ºC high-κ layer but not the as-deposited film, which show serious hysteresis in its *CV* characteristic. This suggest that the stress induced traps in the high-κ layer could have a different nature from the trap responsible for *CV* hysteresis.

References

[1] Robertson, Rep. Prog. Phys. 69, 327, (2006)
[2] Molina *et al.*, J Electrochemical Soc., 154 (5), G110 (2007)
[3] Ang *et al.*, Appl. Phys. Lett., to be published
[4] Ong *et al.*, Appl. Phys. Lett., 92, 022904 (2008)
[5] Gougousi *et al.*, J. Appl. Phys., 93, 1691 (2003)

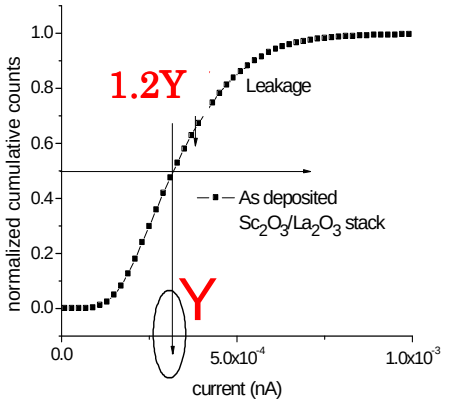

Fig. 1 Definition of leakage current as the current with value 20% above the median (Y) of the current distribution within the scanned area.

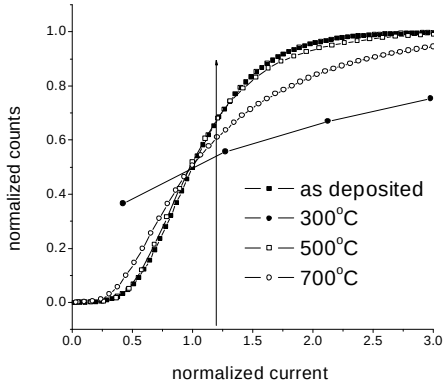

Fig. 3 Current distributions of a scanned 50nmx50nm area for the as-deposited and annealed gate stack.

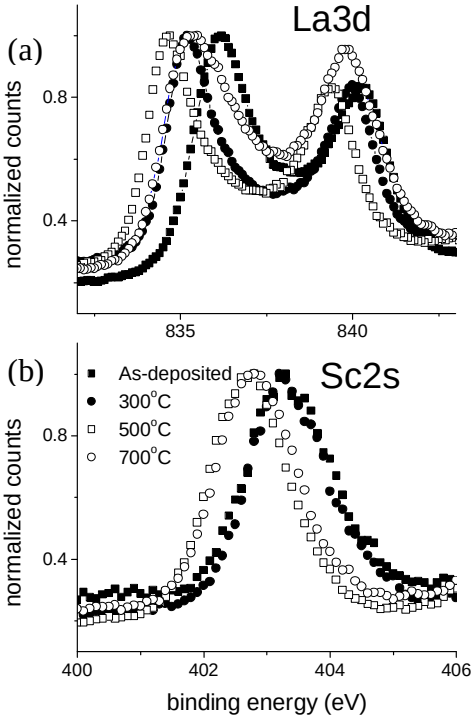

Fig. 4 XPS data showing (a) La3d spectrum and (b) Sc2s spectrum of the gate stacks.

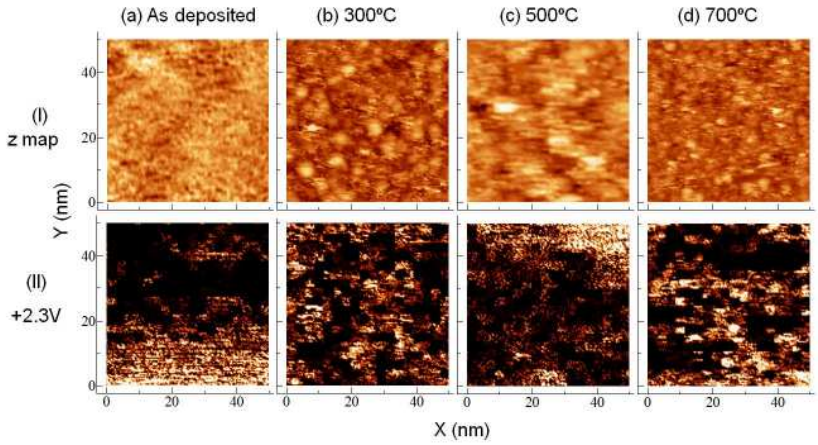

Fig. 2 (I) CCI images, which reflect the surface topography (z). (II) Corresponding CITS current map at +2.3 *Vs* for (a) as-deposited (b) 300ºC (c) 500ºC and (d) 700ºC N_2 annealed Sc_2O_3/La_2O_3 gate stack.

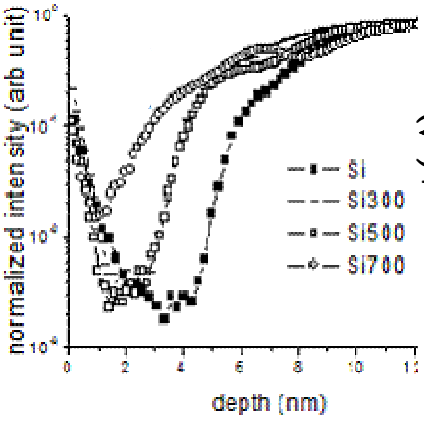

Fig. 5 TOF-sims Si depth profile of the four samples under study. Si back-diffusion is observed to be relatively significant in the 700ºC annealed sample.

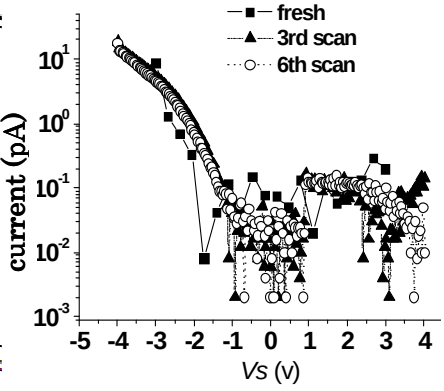

Fig. 6 1st, 3rd and 6th local *IV* of the as-deposited film at a point without pre-existing electronic traps. No increase in leakage current can be observed in the positive *Vs*

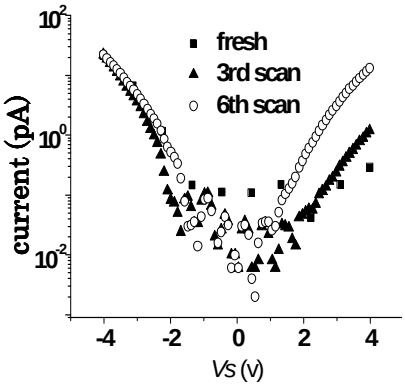

Fig. 7 1st, 3rd and 6th local *IV* of the 500ºC annealed film at a point without pre-existing electronic traps. Positive current increases upon successive scans and gradually exhibit a parallel shift to lower voltages.

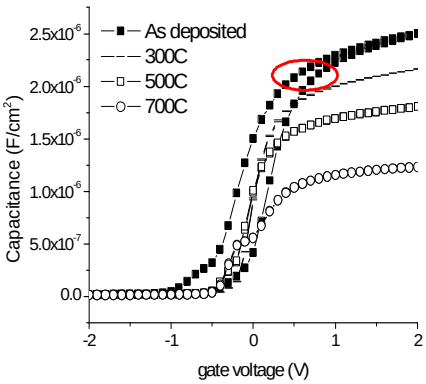

Fig. 8 *CV* of the four samples under study. The area of the capacitors are 100umx100um, with 50nm thick W as gate. Hysteresis is observed for the as-deposited film. Annealing removes hysteresis.