P-1-3

New Observation on PBTI Characteristics of Contact Etching Stop Layer (CESL) Induced Tensile Strained HfO_2 nMOSFET

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1. Introduction

HfO_2 gate dielectrics are considered to be the most promising high-k dielectrics to meet the future ULSI application [1], due to its high dielectric constant and excellent thermal stability [2-3]. Recently, the nitride-cap stressor [4-6] has been used to improve mobility in CMOS technology. However, the reliability issue such as PBTI characteristics of nitride-cap and high-k in CMOS technology has yet to be proposed. In this work, "close-to-intrinsic" improvement of CESL-HfO_2 nMOSFETs were observed using pulse-IV measurement. On the other hand, improved reliability including interface characterization and PBTI characteristics was also found for CESL-devices due to hydrogen passivation and nitrogen incorporation, respectively.

2. Device Preparation

A 0.35-μm process was used with local-oxidation-of-silicon (LOCOS) isolation. After standard RCA cleaning, 6 nm HfO_2 thin films were deposited. The CETs of HfO_2 thin films were almost the same (1.6nm) for all samples as indicated in Fig.1. Then, α-Si (deposition at 550 ^oC,) of thickness 50 nm was deposited in order to get the local tensile strain n-channel [6], and the final poly-gate thickness was 150 nm. After the S/D formation, a low pressure chemical vapor deposition (LPCVD) silicon nitride (CESL) was directly deposited on the transistor at 780 ^oC with different thicknesses of 50, 100 and 300 nm, and followed by a 200 nm PE-SiO_2 deposition. After contact alignment, the PE-oxide and SiN layer on the S/D regions were etched in the same system. After these processes, a four-level metallization (Ti–TiN–Al–TiN) was carried out in the PVD system for the contact.

3. Results and Discussion

Figure 2 shows the I_D-V_G transfer characteristics of the conventional and CESL strained HfO_2 nMOSFETs, where the device channel length and width were 0.35 and 10 μm, respectively. Negligible DIBL effect (<40 mV) can be observed for conventional and CESL strained HfO_2 nMOSFETs. The "close-to-intrinsic" characteristics of HfO_2 gate dielectrics were analyzed using PIV measurement as shown in Figs. 3-4. The PIV current is larger than DC indicates that charge trapping can be eliminated for PIV operation, as approved in Fig. 3(a). The driving current under PIV operation was enhanced with increasing capping nitride thickness, as indicated in Fig. 3(b). The driving current of the 300 nm SiN-capped device with 0.35 *u*m gate length showed a 60 % increase over the as-deposited device at V_D = 2 V and V_G-V_{th} = 2 V, as shown in Fig. 3. Figure 4 presents the field-effect mobility measured by PIV system at different capping SiN-layer thicknesses. Increased electron mobility with increasing capping SiN-layer thickness is depicted in this figure, and nMOSFETs with CESL 300-nm show a significant mobility increase (55%), by comparison with the as-deposited sample. Therefore, the "close-to-intrinsic" improvement of the characteristics of the CESL-nMOSFETs with HfO_2 gate dielectrics can be obtained in this work by using PIV measurement.

Figure 5 shows PBTI characteristics including (a) V_{TH} shift, (b) I_{OFF}, for all devices. The obvious V_{TH} shift reduction can be observed for the CESL-devices. Furthermore, comparison with the as-deposited sample, the V_{TH} shift decreased with increasing the CESL thickness as shown in Fig. 1(a). Figure 1(b) indicates that the Idsat degradation also decreases with increasing CESL thickness, which can be speculated to the incorporation of N-containing precursors (NH_3) during the SiN deposition step, and the nitrogen species tend to eliminate some defect states of HfO_2 thin film, resulting in less charge trapping during PBTI stress. As a result, both the V_{TH} shift and Idsat degradation can be much improved for the CESL-devices. The I_{OFF} and g_m are almost the same during 1000s PBTI stress for all samples, as described in Fig. 6. It means that PBTI only affects on bulk HfO_2 thin film, instead of HfO_2/Si interface. The relationship between interface characterization and PBTI for CESL strained HfO_2 nMOSFETs was also demonstrated using charge pumping analysis, as shown in Fig. 7. First, the as-deposited sample (Fig. 7(a)) depicts the larger charge pumping current (I_{CP}) than 300 nm CESL capped one (Fig. 7(b)). The Nit extracted from I_{CP} is only 9×10^{10} cm^{-2} for the 300 nm CESL capped device, while the as-deposited one is 6×10^{11} cm^{-2}. This is ascribed to the use of H-containing precursors (SiH_2Cl_2) during the SiN deposition step. The incorporated hydrogen species tends to passivate the interface states. After 1000s PBTI stress, the I_{CP} increase is only 4 %, and the Nit is almost the same before and after PBTI stress for both as-deposited and 300 nm CESL capped device, respectively. The subthreshold slope is almost the same before and after PBTI stress for both as-deposited and 300 nm CESL capped device (Fig. 8), also indicating that PBTI only affects on bulk HfO_2 thin film of CESL-device. The difference of I_D-V_G curves can be observed between before and after PBTI stress are V_{TH} shift and Idsat degradation. However, both V_{TH} shift and Idsat degradation are decreased with increasing CESL thickness, as mentioned above.

The PBTI characteristics under elevated temperatures were shown in Fig. 9. The V_{TH} shifts increase with increasing temperature for all samples. In addition, the V_{TH} shifts of CESL-devices are almost the same at room temperature and 50 ^oC after 1000s PBTI stress. However, the V_{TH} shifts increase a lot at high temperature (60 ^oC) for CESL-devices, suggesting that the SiN-capped ones has deep electron trap. On the contrary, the as-deposited one shows obvious temperature dependence for V_{TH} shifts during PBTI stress. These results indicated that the nitrogen incorporation effectively passivated the HfO_2 dielectric vacancies, resulting in a deeper trapping cross section and a lower concentration of generated traps. Figure 10 exhibits gate leakage current under inversion mode for all samples. To further investigate the effective charge trapping level of as-deposited and CESL-HfO_2 gate dielectrics, the Frenkel-Poole (F-P) conduction fitting is performed, as shown in Fig. 11. The extracted trap energy (Φ_B) under substrate injection for the 300 nm SiN-capped device is 0.83 eV from the conduction band of HfO_2, while that of the as-deposited sample is about 0.75 eV. As the CESL thickness increases, the increase in the effective trapping level is easily observed, meaning that most of the shallow traps in HfO_2 film can be eliminated using this CESL strain technique due to nitrogen incorporation. Figure 12 demonstrates charge trapping mechanisms for (a) as-deposited (0.75 eV), and (b) CESL HfO_2 nMOSFET (> 0.8 eV), respectively.

4. Conclusion

For the first time, new observation on SiN-cap strain-induced improved characteristics and PBTI reliability of HfO_2 nMOSFETs was investigated. The "close-to-intrinsic" characteristics can also be demonstrated for SiN-capped HfO_2 nMOSFETs using PIV analysis. The nitrogen incorporation effectively passivated the HfO_2 dielectric vacancies, resulting in a deeper trapping level (0.83 eV) and better PBTI reliability for CESL-devices. These results provide a valuable guideline for future 32 nm and beyond CMOS device designs with high-k and strain engineering.

Reference

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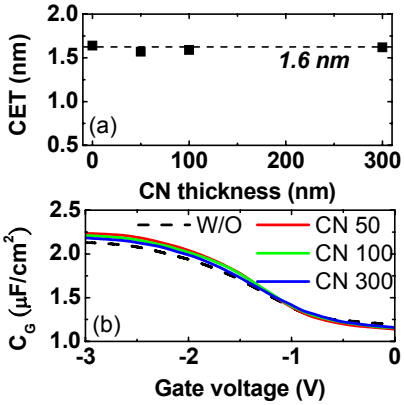

Fig.1. (a) CET of all HfO_2 thin films, extracted from (b) C-V curves of all samples.

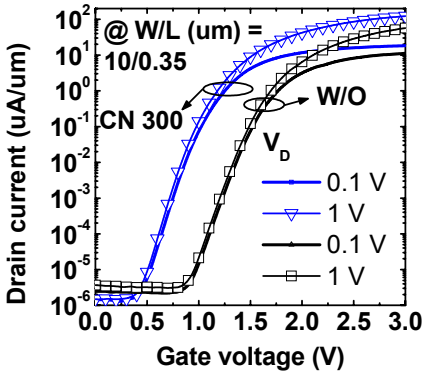

Fig.2. The I_D-V_G characteristics of as-deposited and CESL (300 nm) HfO_2 nMOSFETs.

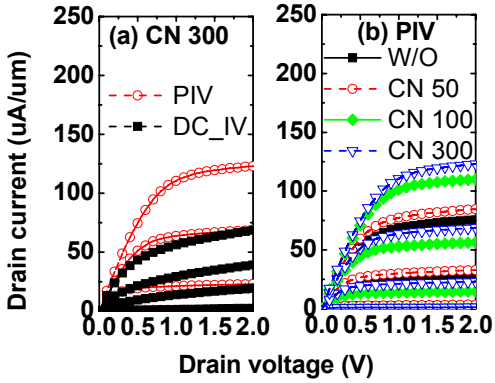

Fig.3. The I_D-V_D characteristics of (a) 300 nm CESL-device under DC and pulse-IV measurement, and (b) all samples under pulse-IV measurement.

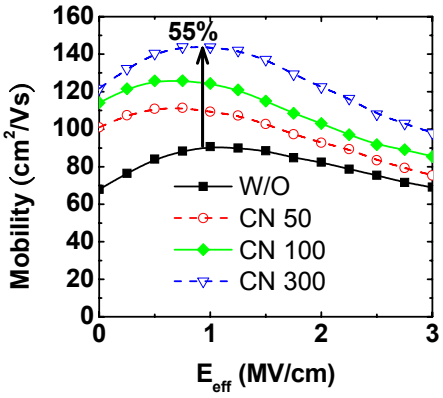

Fig.4. The electron mobility increases for CESL strained HfO_2 nMOSFETs, compared to as-deposited one.

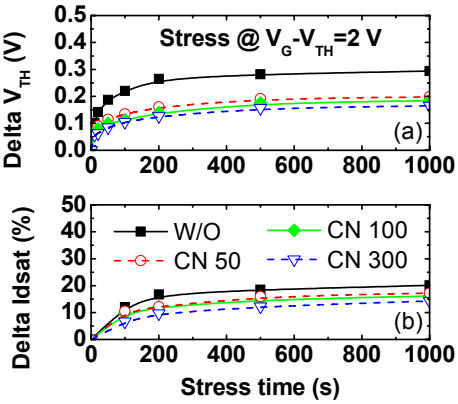

Fig.5. (a) V_{TH} shift, and (b) delta Idsat for all samples under PBTI stress.

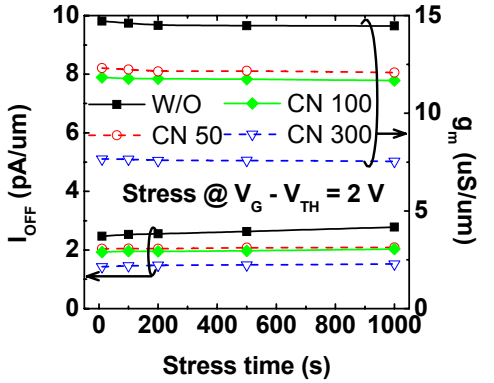

Fig.6. I_{OFF} and G_M are almost the same during PBTI stress for all samples.

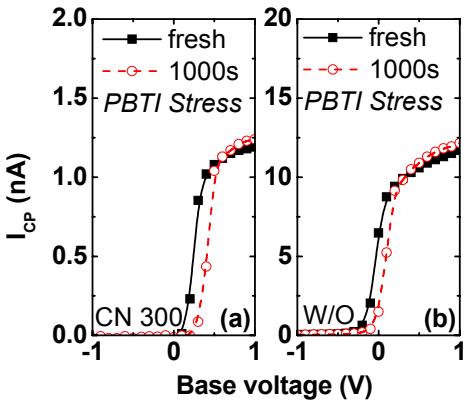

Fig.7. Charge pumping current before and after 1000s PBTI stress for (a) as-deposited, and (b) 300 nm CESL samples, respectively.

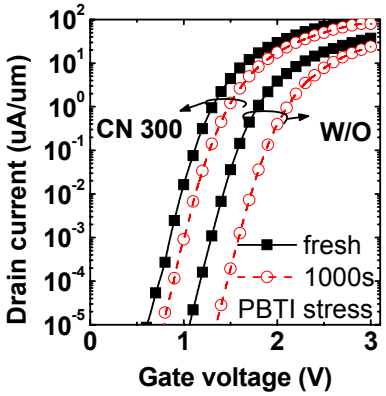

Fig.8. I_D-V_G curves before and after 1000s PBTI stress for (c) as-deposited, and (d) 300 nm CESL capped device

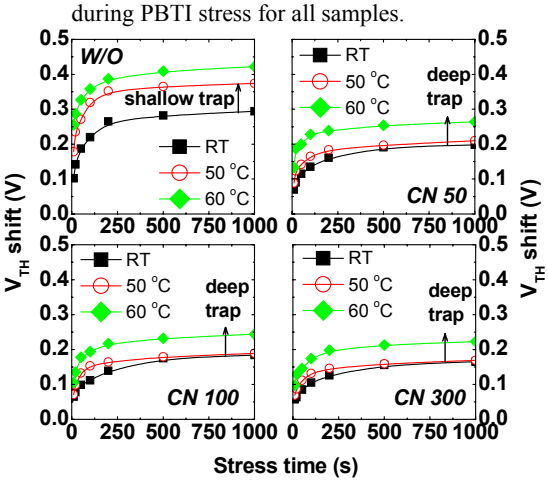

Fig.9. PBTI characteristics (@V_G – V_{TH} = 2V) under different temperatures for all samples.

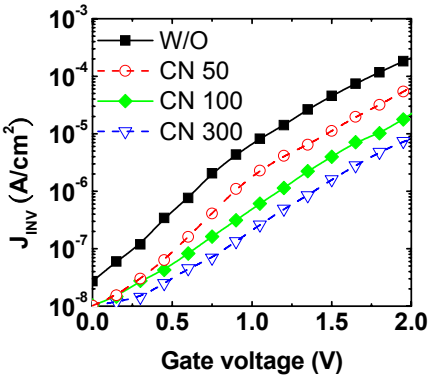

Fig.10. The gate leakage currents under substrate injection (inversion mode) for HfO_2 nMOSFETs.

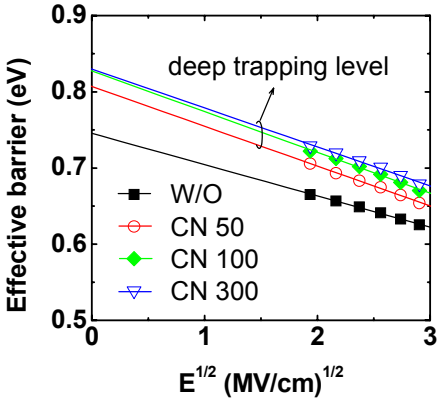

Fig.11. The well F-P curve fitting $J = E_{OX} \times \exp\left\{-q\left[\Phi_B - \left(qE_{OX} - \pi\varepsilon_i\right)^{1/2}\right]/kT\right\}$ for inversion currents of all samples.

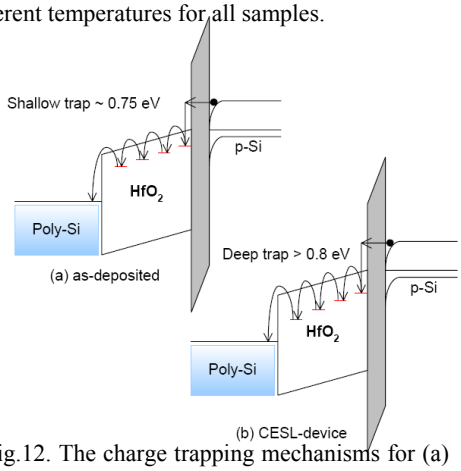

Fig.12. The charge trapping mechanisms for (a) as-deposited, and (b) CESL HfO_2 nMOSFET. The CESL-device has deep electron trap (> 0.8 eV).