Low-Temperature Polycrystalline Silicon Thin-Film-Transistor with Fluorinated High-k HfO2 Gate Dielectrics by HF Dip and CF4 Plasma
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1. Introduction
Recently, high-speed display driving circuits require thin film transistor (TFTs) to operate at low voltages and high driving currents, with a low threshold voltage. Using a thin gate oxide can increase the driving current of TFTs[1]. Therefore, we use hafnium dioxide (HfO2) due to high-k value (~25), widebandgap, acceptable band alignment, and superior thermal stability with poly-Si[1]. However Low-Temperature Polycrystalline Silicon (LTPS) TFTs with high-k gate dielectric would suffer from a more undesirable gate-induced drain leakage (GIDL) current. To address this GIDL issue, application CF4 plasma on poly-Si film, have been applied to effectively improve the device performance by reducing the trap state densities[2]. Besides native oxide on poly-Si film will increase the interface roughness, gate oxide leakage current. We have used HF dip to reduce of native oxide[3].

2. Experiment
Fig. 1 illustrates the key fabrication steps for the proposed HfO2 LTPS TFTs. The fabrication started by depositing a 70 nm amorphous Si (α-Si) layer at 550°C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers capped with a 600 nm thick thermal oxide layer. The deposited α-Si layer was then recrystallized by the SPC process at 600 °C for 24 h in N2 ambient. The individual active region was patterned and defined. Then the four conditions of surface treatments applied on the recrystallized poly-Si film in table I. Afterward, a 20 nm HfO2 film was deposited to serve as the gate dielectric by sputter system, followed by a re-alignment of rapid thermal anneal (RTA) at 600°C for 30 s in N2 ambient to improve the gate-dielectric quality. Next, a 200 nm thick poly-Si was deposited and patterned for the gate electrode. After a self-aligned phosphorous ion implantation was performed at 30 keV to a dose of 5 × 1015 cm-2 to dope the source/drain regions, the dopant was activated by the thermal budget of 600 °C for 12 h. After a 200 nm passivation SiO2 layer was deposited by PECVD at 300 °C, the contact holes were patterned by a two-step etching process. The 200 nm oxide layer and 20 nm HfO2 layer were etched by BOE solution and RIE, respectively. Finally, a typical 600 nm Al metallization was performed, followed by 400 °C sintering in the thermal furnace.

3. Results and Discussion
I. Typical Characterisation of TFPs
Fig. 2 shows the current density vs gate voltage (J-V) characteristics of four conditions. The breakdown voltage of conditions CF4 and HF + CF4 was deceased. We suppose the fluorine passivation plays a role in blocking oxygen diffusion into the Si, resulting in an CET reduction for the HfO2 gate dielectrics. Fig. 3 shows typical capacitor-voltage (C-V) characteristic of the MOS capacitor at 100 kHz. The thinner equivalent-oxide thickness (EOT) extracted from C-V curves was obtained for the HfO2 gate dielectrics with HF dip and CF4 plasma treatment. Fig. 4 shows the typical J-V characteristic for HfO2 LTPS TFTs. The drawn channel length (L) and channel width (W) are 5 μm and 50 μm, respectively. Obviously, the driving current of HF + CF4 condition LTPS TFT (about 30 μA) is three times higher than that of control sample LTPS TFT (about 11.8 μA) at VDS = 4 V and VGS = 5 V. Fig. 5 depicts the transfer characteristics of HfO2 LTPS TFTs at VDS = 0.1 V. The measured as well as extracted device parameters are summarized in table II. Therefore, the fluorine passivation of trap states is found to greatly improve characteristics with HF dip and CF4 plasma treatments[3]. Notably, the maximum GIDL current of the HfO2 LTPS TFT with HF dip and CF4 plasma treatments (0.156 nA) is more lower than sample without HF dip and without CF4 plasma treatments (30 nA). This is attributed to two reasons: First, HF dip to reduce interface roughness. Second, the trap states at the grain boundaries can be effectively passivated by the CF4 plasma treatment, leading to an improved electrical performance[2]. Fig 6 exhibits the ln(Ion/(VGs-VFB)) vs 1/(VGS-VFB) curves in the strong inversion at VDS = 0.1V. It is observed with HF dip and CF4 plasma treatments for the reduction of gate boundary trap states.

II. Fluorine Effects on the Reliability of TFTs
We can observe low field-effect mobility (μ) with HF dip in table II, we suppose it is attributed to interface roughness and high-k dipole, resulting scattering effect. The S.S. and trap-states greatly improved by using HF dip and CF4 plasma treatment due to fluorine incorporation at the HfO2/poly-Si interface. Fig. 9 illustrates the strong Si-F bonds replace the dangling bonds for the fluorinated poly-Si film by CF4 plasma treatment.

III. Mechanism of the Fluorine Passivation on Grain Boundary
We can observe low field-effect mobility (μ) with HF dip in table II, we suppose it is attributed to interface roughness and high-k dipole, resulting scattering effect. The S.S. and trap-states greatly improved by using HF dip and CF4 plasma treatment due to fluorine incorporation at the HfO2/poly-Si interface. Fig. 9 illustrates the strong Si-F bonds replace the dangling bonds for the fluorinated poly-Si film by CF4 plasma treatment.

4. Conclusions
The HfO2 LTPS TFT with HF dip and CF4 plasma treatments exhibit better electrical properties including VTH, field-effect mobility, S.S., on-state characteristics and Ion/Ioff. In conclusion CF4 plasma on poly-Si film, have been applied to effectively improve the device performance by reducing the trap state densities.

Acknowledgements
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References
Table I. Four process conditions of Poly-Si surface treatments.

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<tr>
<th>Condition</th>
<th>V_{ox} (V)</th>
<th>EOT (nm)</th>
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<tr>
<td>Control</td>
<td>5.98</td>
<td>1.41</td>
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<tr>
<td>CF4</td>
<td>5.43</td>
<td>1.39</td>
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<tr>
<td>HF</td>
<td>5.86</td>
<td>1.44</td>
</tr>
<tr>
<td>HF+CF4</td>
<td>4.92</td>
<td>1.36</td>
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</table>

Table II. Device parameters for poly-Si HfO2 TFTs with various surface treatment at V_{DS} = 0.1 V.

<table>
<thead>
<tr>
<th>Sample</th>
<th>V_{gs} (V)</th>
<th>S.S. (V/dec)</th>
<th>I_{ds} (mA)</th>
<th>t_{max} (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>4.6</td>
<td>0.17</td>
<td>4.99</td>
<td>0.0443</td>
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<tr>
<td>CF4</td>
<td>3.05</td>
<td>0.17</td>
<td>2.33</td>
<td>2.08</td>
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<tr>
<td>HF</td>
<td>3.05</td>
<td>0.17</td>
<td>0.027</td>
<td>0.0137</td>
</tr>
<tr>
<td>HF+CF4</td>
<td>2.0</td>
<td>0.17</td>
<td>4.99</td>
<td>0.67</td>
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</table>

Fig. 1 The schematic cross-section for HfO2 LTPS TFT.

Fig. 2 The J-V characteristics of the variation surface treatment on poly-Si films for the top gate applied with a positive bias.

Fig. 3 Typical C-V characteristics of the MOS capacitor with a HfO2 gate dielectric.

Fig. 4 Output characteristics of the LTPS TFTs using HfO2 as gate dielectric.

Fig. 5 Transfer characteristics of the HfO2 LTPS TFTs with various surface treatments at V_{DS} = 0.1V.

Fig. 6 The grain-boundary trap-states of the various surface treatment conditions.

Fig. 7 (a) Control (b) HF+CF4 of transfer characteristics of the HfO2 LTPS TFTs before and after 1000s stresses at 25℃.

Fig. 8 (a) Control (b) HF+CF4 of output characteristics of the HfO2 LTPS TFTs before and after 1000s stresses at 25℃.

Fig. 9 Illustrates the strong Si-F bonds replace the dangling bonds by CF4 plasma treatment.