Interfacial and Electrical Characterization in MOSFETs with CeO$_2$ Gate Dielectric

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1. Introduction

Aggressive scaling of gate oxide thickness in CMOS transistors for higher performance and circuit density aggravates the problems of gate leakage current and gate dielectric reliability. To overcome these issues, there has been much interest in high-k materials as the potential gate dielectrics beyond sub-45 nm technology nodes [1]. Recently, among various high-k dielectrics studied, CeO$_2$ has emerged as a potential candidate for high-k dielectric applications. The reported advantages of CeO$_2$ include the relatively high dielectric constant (20-26) [2] and the small lattice mismatch with silicon ($\Delta a = 0.35\%$) [2] and the satisfactory thermal stability [3]. Therefore, CeO$_2$ is considered a potential candidate for future gate dielectrics. Because the interfacial property between gate oxide and silicon substrate is a key consideration in CMOS transistors, the energy distribution of interface traps density ($D_{it}$) and the effective capture cross section at the CeO$_2$/Si interface were studied in this work.

2. Experiments and Results

In this work, (100) $p$-type silicon wafers (1-5 $\Omega$-cm) were used as the starting material. Following the standard cleaning procedures and HF dip, the source and drain areas were defined by wet etching and doped by P diffusion. The CeO$_2$ thin film was then deposited by RF magnetron sputtering in Ar at room temperature. The PDA was performed at 500 $^\circ$C in N$_2$ for 60 s. The Al electrodes were deposited using reactive DC magnetron sputtering and patterned by a wet etching process using H$_3$PO$_4$. The PMA was performed at 400 $^\circ$C in N$_2$ for 3 min. The $I-V$ and $C-V$ characteristics were measured by Keithley 4200, HP 4284A, Agilent 81101A and Agilent 4156C.

Fig. 1 shows the quasi-static (QS) and high frequency (1M Hz) $C-V$ curves. The determined dielectric constant ($\kappa$) and EOT were about 23 and 1.9 nm, respectively. The flat band voltage shift ($\Delta V_{FB}$) of the two high frequency sweeps was about 14 mV, which indicates that the CeO$_2$ gate dielectric have acceptable hysteresis phenomenon. The $D_{it}$ can be extracted in the depletion region where the $C-V$ curves are deviated. High-low frequency $C$-$V$ method is a good way to extract the $D_{it}$ values because the lateral non-uniformity effect [5] can be eliminated. Therefore, the energy distribution of interface traps density was determined by using Eqs. (1) and (2) in Table I, as shown in Fig. 2. The mean $D_{it}$ was evaluated about $8.5 \times 10^{10}$ cm$^{-2}$eV$^{-1}$ from Fig. 2.

Fig. 3 shows the $I_{DS}$-$V_{DS}$ characteristics. The subthreshold swing (SS) was about 66.7 mV/decade. Hence, low $D_{it}$ at the CeO$_2$/Si interface [4] was obtained. The $I_{on}/I_{off}$ ratio was about 10$^7$. It implies that the CeO$_2$ gated MOSFETs have a good current switch. In addition, the $I_{DS}$-$V_{DS}$ characteristics of the CeO$_2$ gated MOSFETs showed the good driving current capability, as plotted in the inset of Fig. 3. Fig. 4 (a) shows the rise/fall time dependence of the charge pumping current ($I_{cp}$) for the CeO$_2$-gated nMOSFETs. The $N_{sh}$ was determined about $3.4 \times 10^{10}$ cm$^{-2}$ at 1MHz and $t_c = t_f = 10$ ns using Eq (3) in Table I. Fig. 4 (b) shows the plot of $I_{cp}/f$ versus $ln(t_c)$ in the inset of Fig. 3. Fig. 4 (a) shows the rise/fall time dependence of the effective capture cross section at the CeO$_2$/Si interface were studied in this work.

3. Conclusions

In this work, MOS capacitors and MOSFETs with CeO$_2$ gate dielectric were fabricated and investigated. The $N_{sh}$, $D_{it}$, $\sigma_n$ and energy distribution of interface traps were characterized using the low-high frequency $C$-$V$ method and charge pumping technique. Experimental results showed that $\sigma_n$, $\sigma_p$, and $\sigma_s$ at the CeO$_2$/Si interface were about $6.3 \times 10^{16}$ cm$^{-2}$eV$^{-1}$, $2.4 \times 10^{10}$ cm$^{-2}$eV$^{-1}$, and $1.1 \times 10^{13}$ cm$^{-2}$eV$^{-1}$, respectively. The $N_{sh}$ and $D_{it}$ of the CeO$_2$ gate MOSFETs are much smaller than those of other high-k-gated MOSFETs and smaller than those of other high-k-gated MOSFETs.

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Fig. 1. The quasi-static and high-frequency (1 M Hz) C-V curves.

Fig. 2. Energy distribution of the interface traps density. $E_0$ and $E_r$ are the traps energy level and intrinsic Fermi level, respectively.

Fig. 3. The $I_{DS}$- $V_{GS}$ characteristics at $V_{DS} = 50$ mV. The inset shows the $I_{DS}$-$V_{GS}$ characteristics.

Fig. 4. (a) Rise/fall time dependence of the $I_{DS}$ for fixed rise time at 200 ns. (b) Rise time dependence of the $I_{DS}$ for fixed fall time at 200 ns. (c) $Q_{DS} (I_{DS})$ as a function of $\ln(t_{r}/t_{f})^{1/2}$ provides the $\sigma_i$ and the $D_{i}$, Trapezoidal wave form was used in this work.

Fig. 5. (a) Fall time dependence of the $I_{DS}$, (b) Rise time dependence of the $I_{DS}$ for fixed fall time at 200 ns. (c) $Q_{DS} (I_{DS})$ as a function of $\ln(t_{r}/t_{f})^{1/2}$ provides the $\sigma_i$ and the $D_{i}$.

Fig. 6. Energy distribution of interface traps as extracted by rise/fall time dependence of $I_{DS}$ for CeO$_2$-gated nMOSFETs from Figs. 5 (a) and (b).

Table 1. A comparison of interfacial properties with SiO$_2$, HfO$_2$, HfSiON, ZrO$_2$ and CeO$_2$ (this work) gate dielectrics.

Reference