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# Instability of Threshold Voltage under DC Drain Bias Stress in Pentacene-based Organic Thin Film Transistors

Ching-Lin Fan[1,2], Tsung-Hsien Yang[1], Chang-Chih Lin[1], and Chin-Yuan Chiang[1]

[1] Department of Electronic Engineering, National Taiwan University of Science and Technology,
43 Sec. 4, Keelung Road, Taipei 106, Taiwan
[2] Graduate Institute of Electro-Optical Engineering, National Taiwan University of Science and Technology,
43 Sec. 4, Keelung Road, Taipei 106, Taiwan
Phone: +886-2-2737-6374 E-mail: clfan@mail.ntust.edu.tw

## 1. Introduction

Organic thin-film transistors (OTFTs) have attracted much attention due to their low-temperature and low-cost fabrication process. Their possible applications are flat-panel displays, electronic papers, radio-frequency identification tags (RFIDs) etc [1-3]. OTFT performance has been significantly improved in the last few years and is comparable to that of the amorphous silicon thin-film transistors (α-TFTs) [4,]. However, the performance stability of OTFT is the key issue for mass production and commercialization. It has been reported that the performance degradation of OTFT includes hydroxyl radicals trapped at grain boundary [5,6], oxygen doping in the organic semiconductor [7,8], charge trapping at the interface state or inside the insulator [9,10], water vapors in the insulator [10], bipolaron formation by accumulated holes [11], leakage current through the gate dielectric [12] and so on. On the other hand, it has been reported that the OTFTs exposed to atmosphere and/or prolonged stressing of gate bias will result in the performance degradation of pentacene-based OTFT in terms of field effect reduction, threshold voltage and subthreshold slope variation [4,13]. However, in our knowledge, the drain bias dependence on the electrical characteristics stability of pentacene-based OTFT has never been reported. Thus, in this study, we investigated the stability of pentacene-based OTFT under dc drain bias stress, especially in threshold voltage shift.

## 2. Experimental

The bottom-contact (BC) configuration of pentacene-based OTFTs were fabricated onto a highly doped n-type Si wafer (resistivity < 0.020 ohm-cm, 500 μm-thick) acting as the gate electrodes. The pentacene-based OTFT configuration is shown in Figure 1. Thermally grown 100 nm-thick $SiO_2$ was used as the gate insulator and the Cr/Pt (2 nm/70 nm) were evaporated using an Electron-Beam evaporation system as Source/Drain (S/D) electrodes. The lift-off method was used to pattern the electrodes onto the $SiO_2$ and then the pentacene was deposited onto the $SiO_2$ as the active layer material. The substrate temperature was kept at 70 ºC. Pentacene film at a thickness of 100 nm was deposited at a rate of 0.1 ~ 0.3 Å/s. The device's channel width (*W*) and channel length (*L*) were around 200 μm and 50 μm, respectively. The electrical measurement was performed using an Agilent HP 4156A semiconductor parameter analyzer in the dark and atmosphere at room temperature.

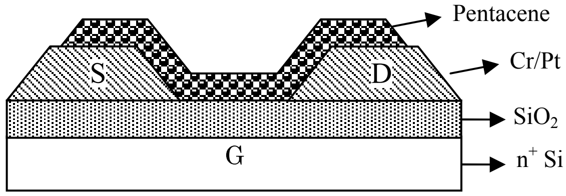


Fig. 1 Schematic diagram of pentacene-based OTFTs with bottom-contact configuration.

## 3. Results and Discussion

Fig. 2 shows the change in the typical transfer curves of pentacene-based OTFTs under storing in the atmosphere for a period time. After 1 hr exposure to ambient air, it is obvious that the on-current ($I_{ON}$) decreased from $2.51 \times 10^{-6}$ to $1.33 \times 10^{-6}$ A, off-current ($I_{OFF}$) increased from $2.20 \times 10^{-12}$ to $4.26 \times 10^{-12}$ A, and threshold voltage ($V_{th}$) increased from -2.5 to -21 V. The $V_{th}$ was calculated from the plot of $I_{DS}^{1/2}$ against $V_{GS}$. The dependence of $V_{th}$ and exposure time to ambient air is inserted in the Fig. 2. We believed that the $O_2$ and $H_2O$ was adsorbed by pentacene film and filled the crevices between the pentacene grains, increasing the concentration of traps, resulting in the increased $V_{th}$ and thus the performance degradation of pentacene-based OTFTs [5-8].

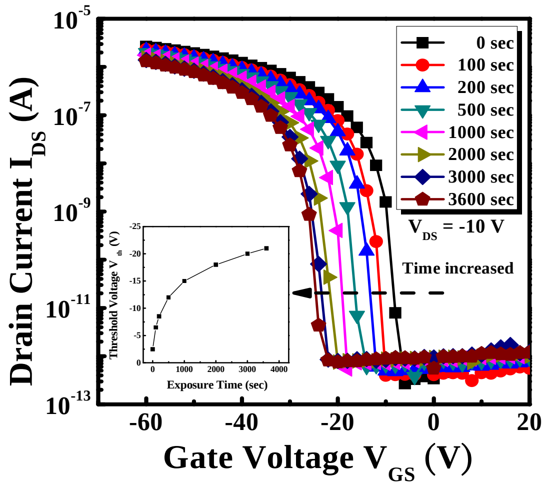


Fig. 2 Typical transfer curves ($I_{DS}$-$V_{GS}$) variations during 1 hr for the pentacene-based OTFTs exposure to ambient air. The inset shows the dependence of $V_{th}$ of the device on exposure time (sec).

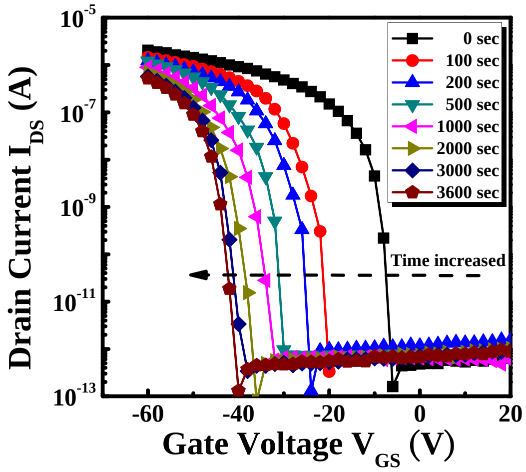


Fig. 3 Typical transfer curves ($I_{DS}$-$V_{GS}$) variations during 1 hr for the pentacene-based OTFTs under drain bias stress at $V_{DS}$ = 30 V in atmosphere.

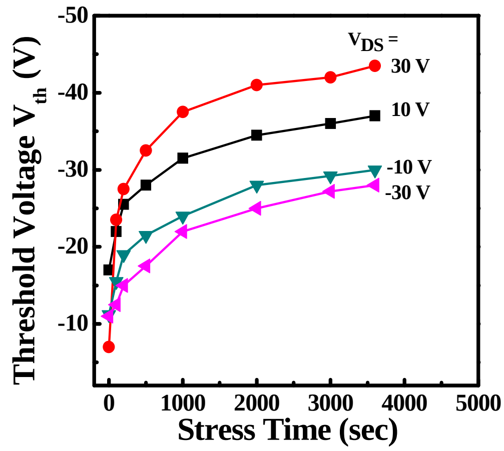


Fig. 4 Threshold voltage ($V_{th}$) variations as a function of stress time at different $V_{DS}$.

Fig. 3 shows the change in typical transfer curves of pentacene-based OTFTs stressed at $V_{DS}$ = 30 V in atmosphere. It is obvious that the $I_{ON}$ decreased from 2.05 × $10^{-6}$ to 5.23 × $10^{-7}$ A and $V_{th}$ increased from -11 to -28 V. The Fig. 4 shows the different drain bias voltage as a function of stress time, stressed at $V_{DS}$ = 30 V in atmosphere. It indicates that the drain bias was applied in positive or negative bias voltage and the $V_{th}$ degradation is less than that applied in positive bias voltage. We believe that the increasing trap state density due to the adsorption of $O_2$ and $H_2O$ in the pentacene film and the enhancement of vertical electrical-field are the main reasons. The pentacene is a p-type organic semiconductor and the pentacene-based OTFTs are usually operated in accumulation mode at $V_{GS} < 0$ and $V_{DS} < 0$. Thus, when $V_{DS}$ was applied in positive bias voltage, the width of depletion region in the channel will be increased, resulting in the increased the traps density near drain side in the channel as a result of the adsorbed $O_2$ and $H_2O$ in the pentacene film. On the other hand, the positive drain bias voltage will result in the vertical electric field in the channel larger than that in negative drain bias voltage. Thus, the carrier injection into gate insulator by the increased trap-state density due to the absorption of the $O_2$ and $H_2O$ molecules will be enhanced with the effect of the large vertical electric field. The carrier injection into the gate insulator will result in the increasing extra oxide charges or interface states, existing in the gate insulator or at the interface between gate insulator and channel. Thus, the performances of pentacene-based OTFTs were significantly degraded, especially in the $V_{th}$.

## 4. Conclusions

The electrical characteristics of pentacene-based OTFTs in atmosphere and drain bias stress were investigated. The pentacene-based OTFTs under atmosphere stress was indicated that the $I_{ON}$ from 2.51 × $10^{-6}$ to 1.33 × $10^{-6}$ A, $I_{OFF}$ increased from 2.20 × $10^{-12}$ to 4.26 × $10^{-12}$ A, and $V_{th}$ increased from -2.5 to -21 V. In addition, the pentacene-based OTFTs under drain bias stress caused large $V_{th}$ degradation. The $V_{th}$ increased from -11 to -28 V. We presume that the carrier accumulated and increased the traps density near drain side in the channel and vertical electric field were the mainly factors for the $V_{th}$ degradation.


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