Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 644-645

P-11-3

A low-voltage and low-power consumption CMOS image sensor using pulse-width-modulation scheme for biomedical applications

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1. Introduction

Recently, a great deal of attention has been paid on CMOS LSI-based biomedical sensors especially for *in vivo* sensing and imaging applications [1, 2]. For such implantable devices, low power consumption and low operating voltage are required for the sake of long term *in vivo* operation with battery or wireless electrical power distribution with limited capacity.

We have proposed pulse-width-modulation (PWM) pixel-readout scheme as a powerful solution for the bioimplantable imaging devices with low voltage operation and low-power-consumption and demonstrated fundamental characteristics of a fabricated imager with 128 x 96 pixels [3, 4]. In this work, we describe the architecture of our PWM image sensor in detail to increase the pixel number from 128x96 to 352x288 and discuss some essential issues to improve the sensor performance.

2. Operation Principle of the PWM sensor

Fig. 1 shows pixel circuit and a timing diagram of the proposed PWM imaging scheme. In the PWM sensor, a photodiode voltage V_{PD} is compared with a ramp signal. The timing of digital transition of the comparator depends on V_{PD}. Thus, the photodiode voltage was transformed into pulse width. The capacity of a power supply can be reduced since the comparator consumes electrical power only around their threshold voltages.

In this scheme, signal-to-noise ratio (SNR) is less affected by the reduction of power supply voltage. The benefit comes from low input-referred jitter noise since the in-pixel comparator has a large gain compared with conventional image sensor using source follower circuit its gain is less than one. Fig. 2 shows the sample of the captured image by the prototype PWM sensor [3].

It is generally considered that PWM scheme is disadvantageous from the viewpoint of a pixel size [4]. To shrink the pixel size, we have adopted a 3 transistor/pixel configuration including a one-transistor in-pixel comparator M_{AMP}, as shown in Fig.1. The in-pixel comparator M_{AMP} is always biased during readout period, and the bias current is a main factor of pixel power consumption. We have also proposed and demonstrated a low-power pixel with our PWM sensor based on dynamic operation of in-pixel comparators, and successfully reduced the power consumption in pixel array [5].

3. Design of the PWM sensor

We have designed a PWM sensor with a 0.35μm 2-poly, 3-metals standard CMOS technology. Fig. 3 shows a photograph of the fabricated sensor. The specifications of the PWM sensor chip are summarized in table I. In this design, some improvements were implemented from the prototype sensor [3]. First, we have increased the pixel number from 128×96 to 352×288 which corresponds to Common Intermediate Format (CIF) size. The power-supply voltage was reduced from 1.4V for prototype sensor to 1.2V for the present sensor with an aim of operation with a button-battery.

Second, we have lowered the resistance of the ramp signal line to suppress the effect of the IR drop. The horizontal ramp signal line has a finite resistance. Since, all the bias currents for the pixels in a same row are gathered into the ramp signal line, the ramp signal voltage depends on the horizontal pixel position due to IR drop (Fig. 4). To avoid this readout error of the pixel value, we have to take care of an IR drop at the horizontal ramp signal line while readout period. The error of the ramp signal by $\Delta V_{ramp,IRdrop}$ is denoted as follows. When all the in-pixel comparators are on, the maximum $\Delta V_{ramp,IRdrop}$ appears at the farthest pixel. It is expressed by

$$\Delta V_{ramp,IRdrop,\max} = R_{PIX} I_b \frac{N_X (N_X + 1)}{2}. \quad (1)$$

Note that R_{PIX}, I_b, and N_X are resistance of the ramp signal line for each pixel, bias current for the in-pixel comparator, and the number of the horizontal pixels. Here, I_b is denoted by

$$I_b = \frac{f_r N_Y C_{sig} (V_{DD} - V_{ramp,\min})}{\alpha}. \quad (2)$$

Where f_r, N_Y, C_{sig} are frame rate, number of vertical pixels, and parasitic capacitance of the vertical signal line. We assume that the ADC period is equal to the one-horizontal period. α means the rate of the transition period of the comparator. It is denoted by

$$\alpha = \frac{V_{DD} - V_{ramp,\min}}{\Delta V_{ramp} A_V}. \quad (3)$$

To suppress the error smaller than 1/2 LSB, we have to lower the wiring resistance of ramp signal line in the layout. The maximum acceptable resistance of R_{PIX} is expressed by equation (4). In this work, the ramp signal line consists of parallel-configured metal 1, 2, 3 layers to lower the resistance.

$$R_{PIX} < \frac{1}{N_X (N_X + 1) \cdot f_r \cdot N_Y \cdot C_{sig} \cdot A_V \cdot 2^{N_{ADC}}}. \quad (4)$$

Third, we have improved the bootstrap circuit to suppress the variation of the reset level. The prototype sensor had a bootstrap

circuit to pull up the gate voltage of the reset transistor M_{RST} and the row select transistor M_{SEL} during reset period [3]. It required a larger voltage than $V_{ramp,rst}+2V_{th}$, which is higher than the power supply voltage. The reset transistor M_{RST} couples the clock transitions to the photodiode capacitance through its gate-source overlap capacitance. After the reset period, the bootstrapped voltage drops by the clock feedthrough. The effect of the clock feedthrough causes a variation of the reset level of the photodiode. To suppress the effect of the clock feedthrough, we have also improved the bootstrap circuit to extend the fall time. The time from beginning the fall of the bootstrapped voltage to finishing completely is defined as the fall time. Fig. 5 shows output signals of the previous and the present bootstrap circuit simulated by spice.

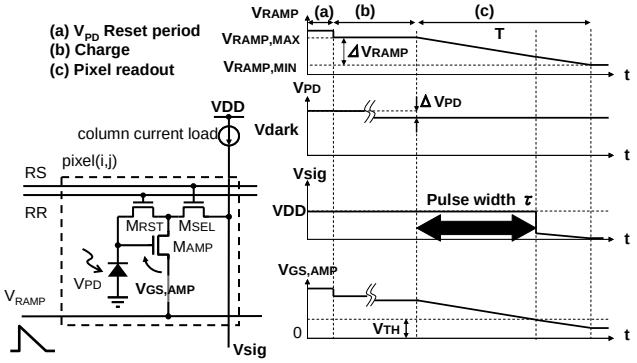

Fig. 1 Pixel circuits of PWM image sensor and the timing diagram

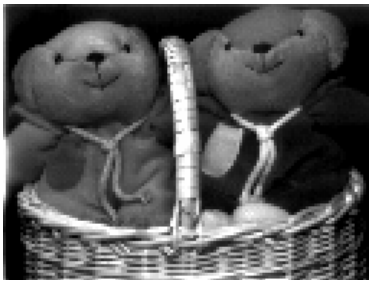

Fig. 2 Captured image by the prototype PWM sensor (1.4V)

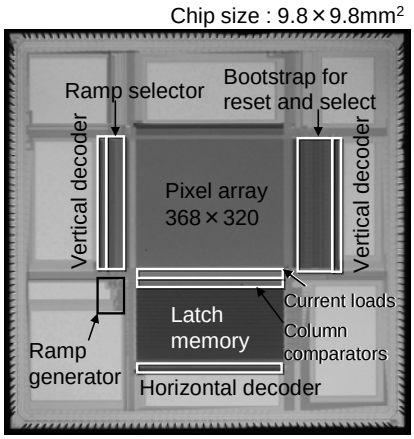

Fig. 3 The fabricated PWM image sensor

Table I Specifications of PWM sensor chip

Technology	0.35 μm 2P3M CMOS
Chip size	9.8 x 9.8mm^2
Pixel count	368×320 (CIF)
Pixel size	10μm x 10μm
Frame rate	30 fps
Fill factor	18.5 %
ADC resolution	10 bit
Supply voltage	1.2 V

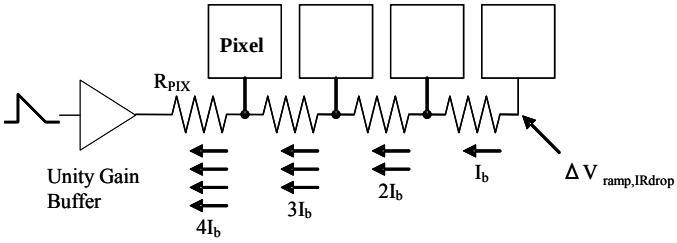

Fig. 4 IR drop at horizontal ramp signal line.

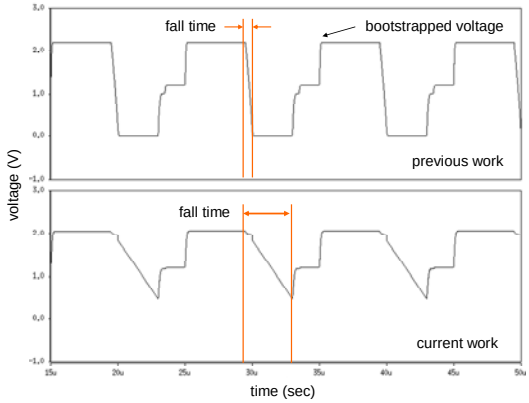

Fig. 5 Spice simulation results of bootstrap circuit output. The upper trace shows the previous work and the lower shows the current work.

4. Conclusions

We have designed and fabricated a CIF ($352^H \times 288^V$ pixels) PWM sensor in a 0.35-μm CMOS technology with a 1.2-V single-power-supply voltage. We also described some design considerations and formulated about IR drop in PWM sensor.

Acknowledgements

The VLSI chip in this study was fabricated in the chip fabrication program of the VLSI Design and Education Center (VDEC) at the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

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