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Design of Logic Module based on Magnetic-Tunnel-Junction Elements for Nonvolatile FPGA

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1. Introduction

A magnetic-tunnel-junction (MTJ) shows potential for a universal logic element which can implement the sequential logic as well as the combinational one, since an MTJ element can compute Boolean functions and also store the output results in itself [1]. The conventional structure for magneto-logic needed triple-layer metal lines over an MTJ element [2]. Fig. 1(a) shows a structure of single-layer (SL) MTJ element proposed in our previous work [3] that provides improved functional flexibility and requires fewer fabrication steps. In this paper, we present a logic module based on MTJ elements which can be used as a basic logic cell for FPGA. S-Module is a basic logic cell for ACT3 family of FPGAs by Actel Inc.[4] It can implement arbitrary five-input logic functions together with a sequential element. We designed an S-Module using SL MTJ elements and verified the functionality. The functional verification has done by HSPICE simulation with a macro-model developed for magneto-logic design.

2. Nonvolatile S-module using SL MTJ

Basic operation concepts of an SL MTJ element

Bistable states of an MTJ element, high (R_H) and low (R_L) resistance states, can be associated with logic '1' and '0', respectively. The logic value can be changed by the direction of the current passing through layer 1 shown in Fig. 1(a). As indicated in Fig. 1(b), the direction of the current is controlled by a current driver which is switched by combinatorial inputs. If more than two of three inputs have logic '1', positive direction current flows through layer 1 and the MTJ gets high resistance state(R_H), and vice versa. The Boolean expression for the output of a current driver with respect to combinatorial inputs is given as eq. (1).

$$OUT = \alpha \cdot \beta + \beta \cdot \gamma + \gamma \cdot \alpha \qquad (1)$$

A sense amplifier (S/A) compares the resistance on the V_+ node with the one on the V. node with positive offset. Thus, the output of S/A is expressed as in eq. (2) for single MTJ on each node and eq. (3) for two serial MTJs on each node(Fig. 2).

$$OUT = W \cdot \overline{Y} \qquad (2)$$
$$OUT = (W + X) \cdot \overline{Y} \cdot \overline{Z} + (\overline{Y} + \overline{Z}) \cdot W \cdot X \qquad (3)$$

Fig. 3 shows a couple of SL MTJs can realize basic logic functions. A single MTJ implements AND, OR,NOR, and NAND by applying appropriate inputs, and two MTJs with a S/A functions as XOR or XNOR. As shown in Fig. 2(b), we can expand MTJ elements attached to a S/A to realize more complex logic as is given by eq. (3) [5], [6].

Embodiments of the Nonvolatile S-module using SL MTJ

In this section, we describe how the ACT3 S-Module can be implemented using SL MTJ elements. The original schematic with a 4-input MUX shown in Fig. 4(a) is transformed into three 2-input MUXes of Fig. 4(b). An S-Module has four data inputs, such as S_1 to S_4, four select inputs, such as A_0, B_0, A_1, B_1, and a clear signal, CLR. The modified schematic has two interim outputs, such as S_5 and S_6, and the final output Q. The Boolean expressions of the outputs are given in eq. (4), (5), and (6).

$$S_5 = (A_1 + B_1)' S_1 + (A_1 + B_1) S_2 = A_1' B_1' S_1 + A_1 S_2 + B_1 S_2 \qquad (4)$$
$$S_6 = (A_1 + B_1)' S_3 + (A_1 + B_1) S_4 = A_1' B_1' S_3 + A_1 S_4 + B_1 S_4 \qquad (5)$$
$$Q = (A_0 \cdot B_0)' S_5 C + (A_0 \cdot B_0) S_6 C = A_0' S_5 C + B_0' S_5 C + A_0 B_0 S_6 C \qquad (6)$$

Serially connected SL MTJ elements can generate the interim outputs, S_5 and S_6, from the four data inputs and two select inputs. S_5 is achieved with four SL MTJ elements having input sets of (0, A_1, S_2), (1, B_1, S_1), (0, A_1, S_1), and (0, B_1, S_2b) as is shown in Fig. 5. MTJ elements with input sets of (0, A_1, S_2), (1, B_1, S_1), (0, A_1, S_1), and (0, B_1, S_2b) implement ($A_1 \cdot S_2$), ($B_1 + S_1$), ($A_1 \cdot S_1$), and ($B_1 \cdot S_2$b), respectively. The output from each element corresponds to each bit W, X, Y, and Z in eq. (3). Thus, S_5 can be obtained by substituting ($A_1 \cdot S_2$), ($B_1 + S_1$), ($A_1 \cdot S_1$), and ($B_1 \cdot S_2$b) for W, X, Y, and Z in eq. (3). S_6 of eq. (5), can be obtained in the same fashion. The final output Q of eq. (6) is generated by the inputs of A_0 and B_0, aforementioned interim outputs of S_5 and S_6, and CLR. It can be realized in similar way by substitution ($A_0 \cdot S_6$), ($C \cdot B_0 + B_0 \cdot S_5 + S_5 \cdot C$), (Cb), and ($A_0 \cdot B_0 + B_0 \cdot S_5b + S_5b\cdot A_0$) for W, X, Y, and Z in eq. (3), respectively. Now a nonvolatile S-module is embodied without a separate sequential element (SE) because each MTJ element inherently works as a nonvolatile storage.

Advantages of the Nonvolatile S-module

An array of S-modules constitutes an ACT3 FPGA that can be configured to implement any arbitrary logic. As every Boolean operation of ACT3 S-module can be mapped into the proposed nonvolatile S-module, any arbitrary logic can be implemented with an array of the MTJ-based S-modules. FPGAs composed of MTJ-based S-modules have several advantages over conventional CMOS-based FPGAs. First, the MTJ-based FPGAs are free from soft error problems because an MTJ-based S-module stores interim data within the MTJ instead of charge-based

memory devices. Secondly, an FPGA using nonvolatile S-modules doesn't suffer from stand-by power consumption since it is completely safe to shut off the supply power during stand-by such that there is no leakage current during stand-by. Finally, enhanced speed is guaranteed when an FPGA restarts after shut-down because nonvolatile S-modules don't need rebooting.

Simulation Results using HSPICE Macro-Model

In our previous work, various characteristics of an MTJ have been modeled as a circuit macro-model that can be integrated with CMOS logic circuits for HSPICE simulation [6]. We designed a test circuit for the non-volatile S-module using this macro-model. Fig. 6 shows output waveforms of the S-module, simulated with HSPICE. It can be observed that the output bits, Q, keep changing in agreement with eq. (6), according to the data inputs S_1 to S_4 and select inputs A_1, B_1, A_0, and B_0, until C clears Q at the end of one period.

3. Conclusions

It is shown that an SL MTJ can be used to implement a non-volatile S-module which is a basic logic cell for ACT3 family of FPGAs. An FPGA using proposed nonvolatile S-module has great merits in various ways. It is free from soft error of SRAM. Power consumption during stand-by can be reduced to zero because it is completely save to shut off the power supply during stand-by. Nonvolatility ensures improved speed when a system needs to restart. Its functionality was verified by HSPICE simulation using a macro-model of an SL MTJ.

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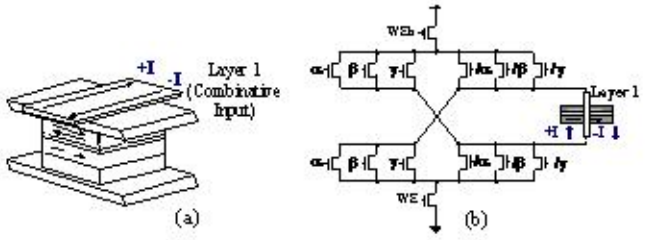

Fig. 1 (a) Structure of an SL MTJ element and (b) schematic of an SL MTJ with a current driver

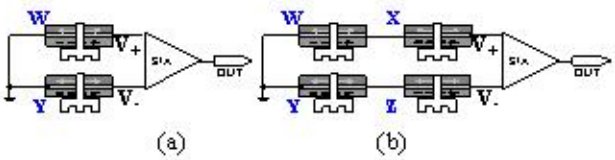

Fig. 2 Schematic of S/A (a) for 2 MTJs and (b) for 4 MTJs.

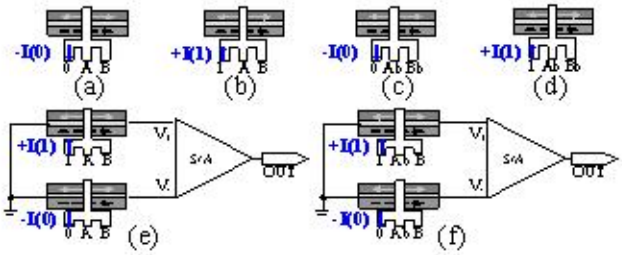

Fig. 3 Magneto-logic gate (a) AND, (b) OR, (c) NOR, (d) NAND, (e) XOR, and (f) XNOR.

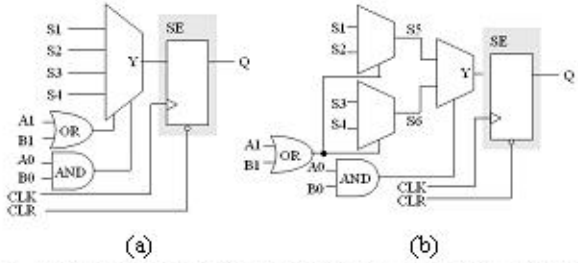

Fig. 4 Schematic of ACT3 S-module (a) using 4-input MUX and (b) using 2-input MUXes

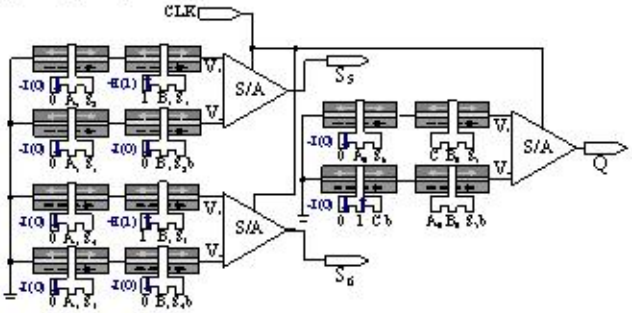

Fig. 5 Schematic of the nonvolatile S-module using SL MTJ

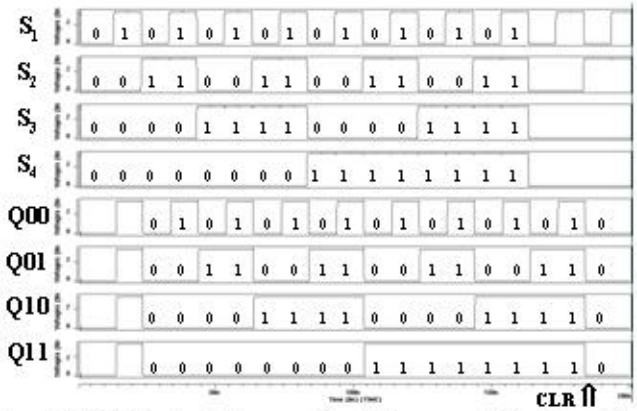

Fig. 6 HSPICE simulation results of the nonvolatile S-module with final outputs Q00, Q01, Q10, and Q11 where the logic sets of select inputs '(A0·B0),(A1+B1)' are '0,0', '0,1', '1,0', and '1,1', respectively.