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Novel Look-Up Table Circuits Using Spin MOSFET

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1. Introduction

Reconfigurable logic has been widely used to reduce a development period of circuit chip and for easy reconstruction of hardware [1]. Field programmable gate array (FPGA) is composed of a large integrated circuit in reconfigurable logic. Look-up table (LUT) circuits play the role of logic in FPGA. Conventional FPGA is based on CMOS technology, which contributes to the progress of electronics. A conventional LUT circuit contains many SRAMs in order to memorize its logic.

We propose a novel LUT circuit using spin MOSFET. Spin MOSFET is composed of ferromagnetic material and semiconductor [2]. Ferromagnetic materials in spin MOSFET contact the source and drain regions, or are used as source and drain regions in the case of ferromagnetic semiconductor. Ferromagnetic material supplies spin and injects spin current through semiconductor. Semiconductor keeps spin information for a long time and has long spin diffusion length [3][4].

Ferromagnetic materials perform a memory function similar to that of hard disk media or magnetic random access memory (MRAM). The magnetization directions affect the current between the ferromagnetic material on source region and that on drain region. Thus I_{DS} of spin MOSFET depends on magnetization directions that show parallel (P) state or antiparallel (AP) state.

We predict that spin MOSFET device can reduce logic circuit area because this device structure includes memory function. Smaller area devices will lead to high-density circuits and high-speed logic circuits owing to the shorter wiring delay.

2. Circuit Design and Simulation

LUT Circuit Using Spin MOSFETs

An LUT circuit memorizes all outputs corresponding to each input. In this structure, memory needs 2^n bit in the case of n inputs. A conventional LUT circuit is composed of 2^n SRAMs and a 2^nx1 multiplexer. A 4-input and 1-output (4x1) LUT circuit, whose structure is widely used in commercial FPGA, contains 96 (=2^4x6) MOSFETs because an SRAM needs 6 MOSFETs. This memory part occupies quite a large area.

We designed the novel LUT circuit using spin MOSFET as shown in Fig. 1. The 16x1 multiplexer in Fig. 1 includes 16 spin MOSFETs. These spin MOSFET devices perform functions of both memory and logic. Output depends on magnetization states (P or AP) in spin MOSFETs.

In the multiplexer, spin MOSFETs are used as logic of least significant bit. The multiplexer is made of both n-type MOSFETs and n-type spin MOSFETs for the sake of pass transistors that show switch function.

During clock signal inputs, current flows through only one spin MOSFET and the current value depends on its magnetization state.

Since Resistance difference between P state and AP state is too short to drive next stage of CMOS gate, a buffer stage is added to output of the multiplexer. LUT circuit without buffer stage will be available if the resistance difference is large enough. The buffer stage is composed of a comparator and a reference part. A conventional sense amplifier used in memory is adopted as the comparator shown in Fig. 1. The reference part contains three n-type MOSFETs and one spin MOSFET whose resistance is adjusted to the middle value between P state and AP state.

The novel LUT circuit selects a spin MOSFET, judges its magnetization state and then outputs high- or low-level voltage.

Number of devices

Circuit area roughly depends on the number of devices. We compare the number of devices between the 4x1 LUT circuit using spin MOSFETs and a conventional circuit based on CMOS technology, as shown in Table I. The conventional LUT circuit contains 166 transistors, whereas the novel LUT circuit using spin MOSFETs contains 49 transistors in the case of 4x1 LUT circuit.

The number of devices is about 1/3 compared with the circuit based on CMOS technology. The novel LUT circuit can substantially reduce the number of devices because the multiplexer includes memory function. It indicates that spin MOSFET has the potential to perform in high density circuit.

This estimation does not take into account the writing operation. Moreover, it does not contain the latch operation at the next stage of the LUT circuit.

Simulations

We simulate the LUT circuit using spin MOSFETs by SPICE simulators (HSPICE and so on). The spin MOSFET model is based on conventional MOSFET parameters using silicon semiconductor with 50nm gate length. Spin MOSFET varies trans-conductance g_m that depends on its magnetization states (P or AP). In SPICE simulator, mobility μ_0 is varied as follows

Table I Number of Devices in LUT Circuits

	Conventional	spin MOSFET
SRAM	96	0
Pass Tr.	70	38
Buffer	0	11
Total	166	49

Here, *MR* is magnetoresistance ratio in spin MOSFET. Thus g_m depends on magnetization states.

These parameter settings are available to confirm basic circuit operations.

Fig. 2 shows simulation results for 2 bits of the novel LUT circuits. The LUT circuit is at first set as OR logic (Fig. 2(a)), and then is written into AND logic (Fig. (b)). *MR* is set to 1000%. Shortest gate length and width are 50nm and 200nm, respectively. This simulation does not take into account surface resistance between magnetic material and semiconductor.

We confirm that the novel LUT circuit operates correctly as shown in Fig. 2. Device parameters can be optimized by simulation. We also confirm that the operation margin depends on *MR* ratio.

The details of circuit parameters and simulation results are described elsewhere [6].

3. Conclusions

A novel LUT circuit using spin MOSFETs is proposed. The number of devices in the LUT circuit is about 1/3 compared with that of the conventional circuit with CMOS technology. Thus, smaller area circuits will be realized, leading to high-density and high-speed circuit. Conventional MOSFET models in SPICE simulators are modified for spin MOSFET. The novel LUT circuit correctly operates in simulation.

Acknowledgements

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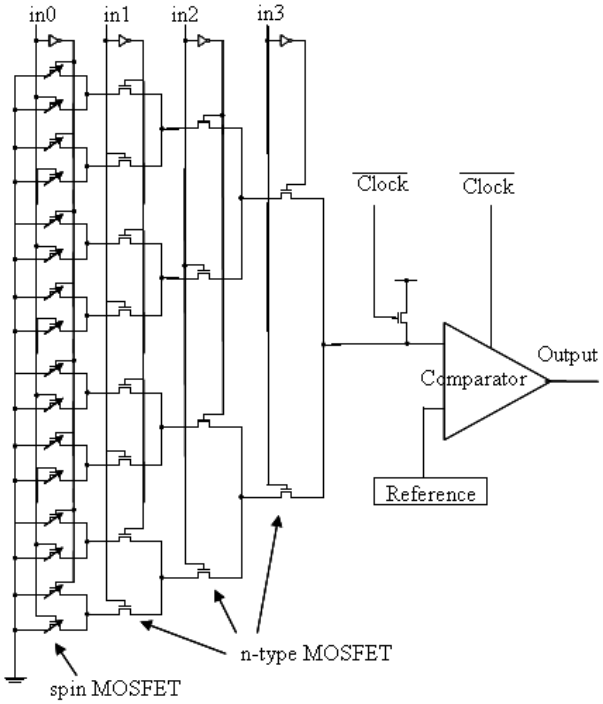

Fig. 1 The novel LUT circuit diagram using spin MOSFETs.

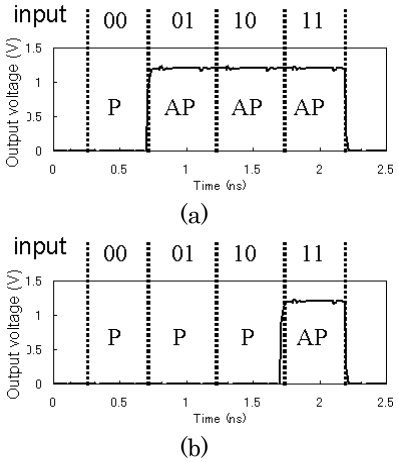

Fig. 2 Simulation results of the novel LUT circuit using spin MOSFETs. P and AP show parallel state and antiparallel state, respectively. (a) OR logic gate (b) AND logic gate.