P-2-8

Copper Plug Barrier Process Optimization for Reliable Transistor Performance

S. K. Manhas. M. Chen, K.D. Buddharaju, H. Y. Li, R. Murthy, S. Balakumar, N. Singh, G. Q. Lo, and D. L. Kwong
Institute of Microelectronics, A-STAR, 11 Science Park Road, Singapore Science Park-II, Singapore 117685
Phone: +65 67705607, FAX: +65 67731914 Email: sanjeev@ime.a-star.edu.sg

I. INTRODUCTION

Copper plug technology is a very viable option for overcoming resistance increase from conventional W-plug process below 0.2um plug sizes [1, 2]. In addition, it also reduces Fab investment by allowing process implementation using existing backend copper interconnects toolsets. However, the device characteristic degradation and reliability is a major concern due to high copper diffusivity resulting in copper induced junction and oxide breakdown. The optimization of the barrier type and its thickness to prevent Cu diffusion is a challenging issue, and can limit the high temperature processes during backend processing. The conventional PVD based tools used to deposit the barrier usually result in poor step coverage creating weak spots for Cu penetration. Previous studies reported a re-sputter approach as a way to alleviate the step coverage issue, but at the added risk of breaching bottom barrier integrity [2, 3]. As a result there is a trade off between as-deposited barrier thickness and plug resistance. Further since the re-sputter process is not very well controlled the minimum sidewall barrier thickness required to prevent Cu diffusion is not very well defined.

In this work we report study of diffusion barrier sidewall thickness needed for different temperatures in 0.2um copper plug technology. The degradation of electrical characteristics of MOSFET and p-n junction diode were used to monitor the Cu penetration in the channel and junctions. Using TaN and TaN+Ta as barrier materials, we show that a ~70Å sidewall barrier is effective in preventing Cu diffusion up to 350ºC/60min, while a minimum thickness of ~100Å is needed for blocking copper diffusion at 420ºC/30min. These results allowed us to determine process window for a reliable 0.2um copper plug technology.

II. DEVICE FABRICATION AND CHARACTERISATION

Copper plug process was implemeted in 0.13µm CMOS technology using 30Å oxide thickness with 0.2µm plugs. As-sputtered thickness details of the different barriers and copper seed layer along with Aluminum contact as reference are given in Table I. The barrier deposition process was implemented using Applied Materials' physical vapour depostion tool with self induced plasma technology. This technolgy allowed to achieve a step coverage of ~30% for conact holes with aspect ratio of 2-3. Fig 1. shows TEM picture of 0.2µm plug with 250Å TaN as-deposited barrier thickness. As can be seen from Fig.1 the sidewall thickness of the barrier is about 70A. The fabricated wafers were subjected to high temperature anneal cycles varying from 200ºC-420ºC to aggravate copper diffusion in the active devices. The effect of thermal stress was minitored in electrical charcteristics of diode off-state current at high reverese bise (6V), MOSFET GIDL current and MOS capacitor leakage in accumation under higher effective field (6.5MV/cm).

III.RESULTS AND DISCUSSION

Figs. 2 shows typical n-MOSFET and p^+-n diode characteristics for 250Å TaN barrier with Cu and Al contact processes (split 1 as reference). It is seen from the Fig. 2(A) that Cu plug shows comparable characteristics like off stage leakage, sub threshold slope and threshold voltage. An improvement of 35% in diode ON resistance was obtained with the Cu plug process as shown in Fig. 3. Fig 4 shows p^+-n diode leakage current distribution with alloy temperature measured at the center and edge of the wafer for Cu plug splits 2, 3 and 4 in Table-1. Fig. 5 shows gate leakage current for 50µm x 50µm MOS capacitors measured under accumulation condition for same split conditions as in Fig. 4. In Fig. 6 the corresponding gate induced drain leakage (GIDL) current distribution measured for NMOFETs with Lg=0.13 µm are shown. It is seen from Figs. 4, 5 and 6 that there is no increase in leakage current for all the barrier thicknesses in splits 2, 3, 4 until 350ºC temperature. However, from diode leakage distribution in Fig. 4, it is seen that split-1 with 250Å as-deposited TaN barrier thickness showed sites with increased leakage current after 420ºC annealing for 30 min. Fig. 6 shows an increase in MOSFET GIDL leakage for this split. Further we note that barrier split with 100Å TaN + 200Ta did not show any diode and GIDL leakage current while an increased gate leakage current was seen. Furthermore, the barrier split condition with 300Å TaN did not show significant increase in any of the measured leakages even up to 420ºC anneal temperature for 30 min.

The leakage observed after 420ºC anneal cycle for split condition 2 (250Å TaN) can be attributed to copper penetration in the junctions leading to formation of copper precipitates [4]. In addition copper migration and formation of copper precipitates at the gate oxide and silicon interface leads to local oxide thinning and higher gate leakages. The formation of these defects can also explain the increased GIDL current as these defects, created near drain-gate junction interface contribute to defect induced tunneling current. Also a component of GIDL is contributed by reverse biased diode leakage in the drain junction. From leakage data in Fig. 4, 5 and 6, it is seen that for 420ºC anneal temperature 100Å TaN + 200Å Ta barrier gives better leakage characteristics than that of 250Å TaN barrier. This can be attributed to the segregation of Nitrogen at grain boundaries in Ta layer thus reducing the channel for copper diffusion [4]. However it is seen that even combined bi-layer thickness of 300Å (split -2) does not provide sufficient barrier to copper diffusion at 420C.

In order to understand the likely copper diffusion path causing device leakage, TEM characterization was done for split with 250Å TaN barrier as shown in Fig. 7. It can be seen from Fig. 7 that there exists a poor barrier coverage at the bottom of the plug, which is due to a notched etch profile. This results in localized thinner barrier, and is attributed to be a weak spot for Cu diffusion at 420ºC temperature cycle causing junction and oxide leakages. The increased barrier thickness for split 4 has sidewall step coverage thickness of ~100Å, which the electrical data of Figs. 4-6 showed is effective in blocking the copper diffusion at 420ºC annealing cycle.

IV. SUMMARY

Copper plug (0.2µm) process with TaN and bi-layer TaN + Ta were implemented in 0.13µm CMOS technology. The barrier effectiveness of the different films were studied as function of plug sidewall barrier thickness and different temperatures cycles. It was shown that effectively 60-70A sidewall barrier thickness can only withstand the temperature of 350ºC for tested time of 60min. The study shows that a sidewall barrier thickness of at least 100Å is needed to stop Cu penetration at 420ºC. Further the TEM analysis showed that insufficient barrier converge at the bottom sidewall corners of the contact plug creates week spots for copper penetration in the device junctions leading to increased leakages.

REFERENCES

[1] M. Inohara et al., IEDM 2001, Tech. Dig., pp. 931-933. [2] G. Van den bosch et al., IEDM 2006, Tech. Dig., pp. 93-96. [3] K. –C. Park et al., Proc. ITC 2003, pp. 165-167. [4] A. A. Istratov and E. R. Weber , J. Electrochem. Soc. Vol. 149, pp. G21-G30, 2002.

Table 1: Cu plug barrier split conditions with different barrier thicknesses, reference split condition 1 had Aluminum deposition with 250A TaN as barrier

Split No	Barrier	Seed	Copper plating thickness
1	250A TaN	Al 2.5kA	-
2	100A TaN + 200Ta	1000A Cu	1500A
3	250A TaN	1000A Cu	1500A
4	300A TaN	1000A Cu	1500A

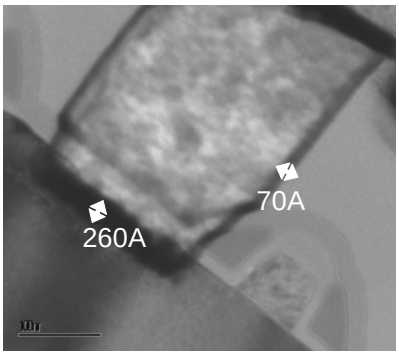

Fig. 1 TEM picture of Cu plug processed wafer with 250A TaN barrier thickness, the side wall thickness was measured to be about 70A.

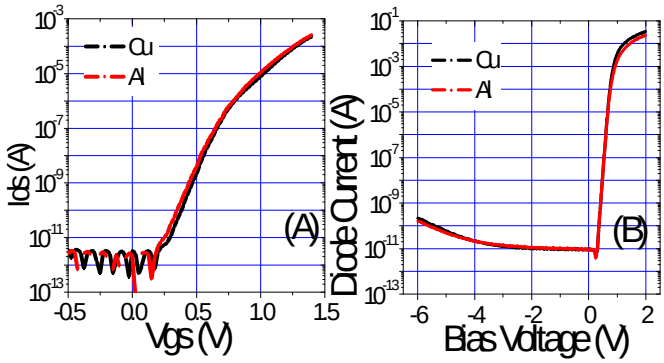

Fig.2 Typical Ids-Vgs (A) and diode current characteristics (B) of Cu plug process with 250A TaN barrier compared to Al contact process.

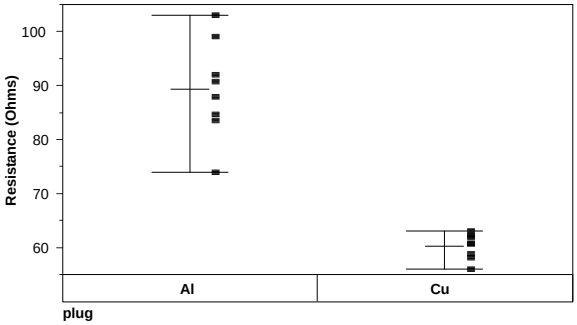

Fig.3 Contact resistance comparison between Cu and Aluminum plugs for 0.2um diameter holes, approximately 35% improvement in contact resistance was obtained.

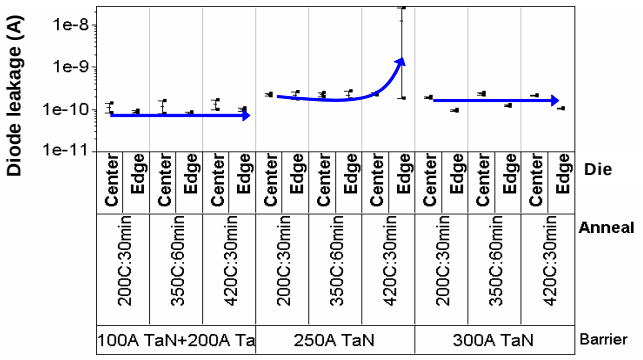

Fig.4 Diode reverse bias leakage distribution (measured at 6V) after 200C, 350C and 420C temperature cycles with different barriers.

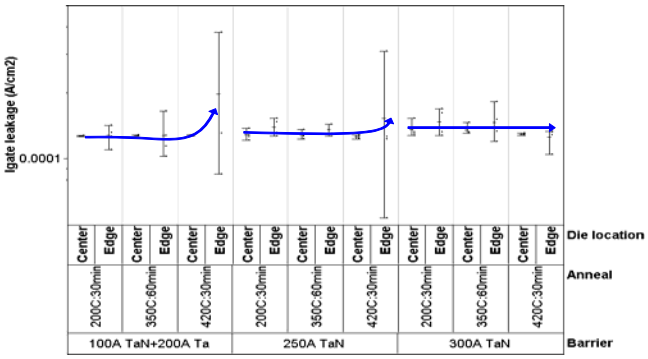

Fig. 5 n+ Gate current leakage distribution measured in accumulation (Vg=-2V) after 200C, 350C and 420C temperature cycles for different barriers.

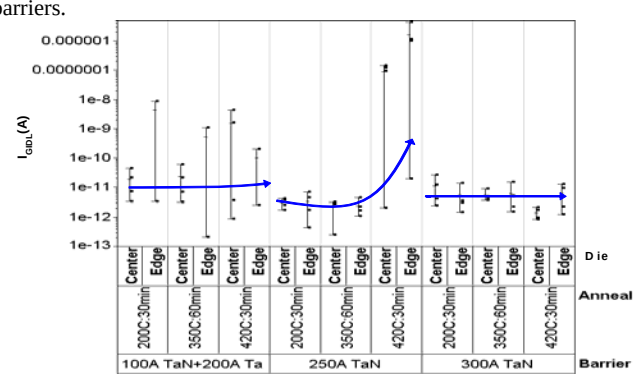

Fig. 6 n-MOSFET GIDL current distribution (measured at Vgs=-0.5V, Vds=1V) after 200C, 350C and 420C temperature cycles for different barriers.

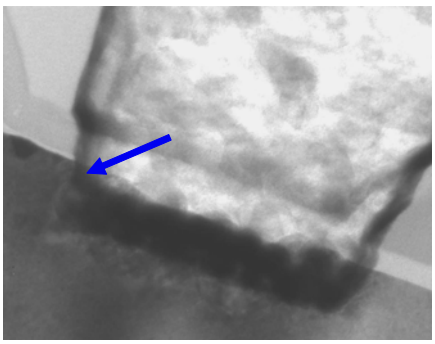

Fig. 7 TEM picture of bottom of barrier coverage for split 2 (250A TaN), the area of poor step converage with likely path of copper penetration is highlighted.