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Experiments and Simulation of Stress Induced Voiding Dependence on Upper Metal Cap Layer in Cu/Low K Interconnects

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1. Introduction

Stress-induced voiding (SIV) effect becomes a reliability concern as metallization technology moving to Cu/low-k interconnects generation [1]. The stress field in interconnects was due to the thermal expansion coefficients (CTE) mismatch between materials. SIV frequently happen at the metal below via and many studies focused on effect due to cap layer of lower metal below via. But effect of cap layer of upper metal is not yet reported. We firstly studied the cap layer effect of upper metal with different material properties. A 3-D Finite Element Analysis (FEA) is used to simulate the stress field inside via test structure under SM tests. TEM analysis was performed on the SM tested structure to confirm the FEA stress results.

2. Experiment

The SIV test is performed on 65 nm generation Cu/low-k dual damascene wafer with monitoring the resistance shift of the test structure at stress temperature of 200^{o} C. Two types of test scheme via structure were presented in Fig. 1. Type a scheme has cap-a layer over metal 3 and type b scheme has cap-b layer over metal 3. The test structure is a M2-VIA2-M3 cross metal via (Fig. 1C) layout. SIV test's sample size is around 50. FEA is achieved by ANSYS software with material properties in table I [2]. Stress free temperature is 300^{o} C.

3. Results and Discussion

Initial resistances are checked without significant difference between these 2 schemes' samples (Fig. 2a). The resistances of some scheme samples had sever shift after 500 hours stress (Fig. 2b). The resistance shift of scheme a samples began at 168 hours. Scheme b samples have relatively stable resistances (Fig. 3). If a typical SM failure criterion is 20% resistance shift, type a scheme process will fail SM qualification, but type b scheme ones will pass. Since type a and type b have the same via structures and metal2/via2 backend interconnect process, type a scheme structure will mislead the stress migration unqualified conclusion on the metal2/via2 interconnect process for this SIV test.

Since Hydrostatic stress S_H is the driving force for stress voiding [3], we first simulated the S_H for both structures. The scheme a structure suffers larger tensile stresses on the surfaces of both upper and lower metal lines than those of scheme b (Fig. 4). S_H on the surface of metal 2 under via is relatively compressive (Fig 5a). The vacancy flux J under S_H influence is given by [4],

$$J = -C\frac{DV}{kT}\nabla S_H, \qquad (1)$$

where D is the diffusion coefficient, V is the atomic volume, and C is the vacancy concentration. Since the stress in other metal line surface is tensile, a large stress gradient will exist there and the vacancy will flux toward metal line surface below via according to (a).

von Mises stress S_V is an index for plastic deformation and dislocation defect, which may contribute to SIV [5]. We found the maximum S_V also located at the metal surface below via (Fig 5b). Both hydrostatic and von Mises stress indicated the metal surface below via is the SIV most vulnerable location. Metal void was found below and around via bottom by TEM analysis (Fig 6). The void location is consistent with the stress analysis results above. Scheme a structure has a 12% larger S_H drop and 17% larger S_V than those of scheme b (Fig 7). The Cu cap layer of scheme a has large CTE difference with Cu (Table I). On the contrary, Cu cap layer of scheme b has similar Cu CTE value. The CTE and other mismatch difference of type a and b schemes contribute their different stress field profile and also the SM performance as shown in above FEA results.

4. Conclusion

The upper metal cap layer's impact on via structure was demonstrated by experiment. The SIV performance is degraded on type a via structure, which has a larger material properties mismatch between upper cap layer and Cu. The stress field inside the structure under this investigation is well profiled. Larger stress field and drop in type a via structures is found. The SIV location from failure analysis is consistent with our FEA stress results.

Reference

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[3] P. A. Flinn, Mater. Res. Bull. **20**, 70 (1995)
[4] J.J. Clement et al., IEEE Trans. Device and Mater. Reliab., vol. 1, no 1. p.33 (2001)
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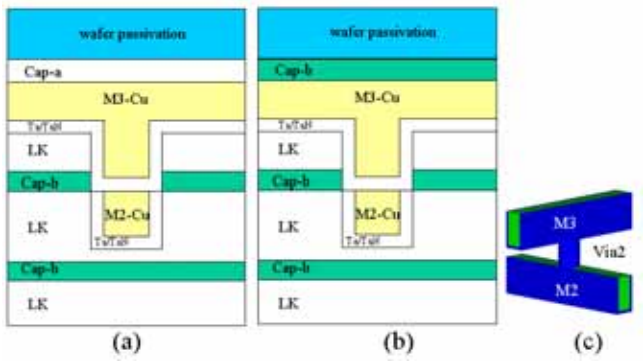

Fig.1: Type of SIV test structure. (a) Cap-type a layer on Metal 3 (b) Cap-type b layer on Metal 3 (c) Cross metal line-via SM structure.

Table I. The material properties used in the FEA [2]

Materials	CTE (ppm/°C)	Modulus(Gpa)	Poisson's ratio
Cu	16.5	125	0.34
Ta/TaN	6.5	185	0.35
Cap-type-a	16	67	0.19
Cap-type-b	1.5	265	0.27
Low K	30	2.5	0.4

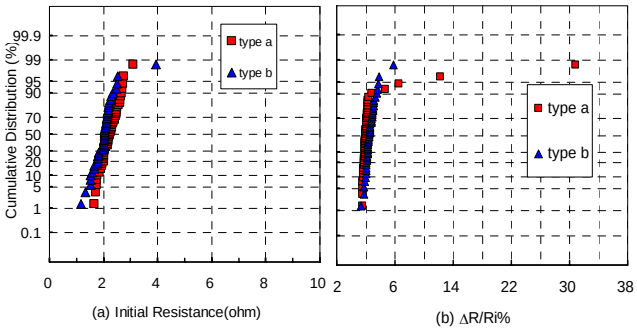

Fig. 2 (a) Initial Resistance and (b) the resistance shift after 500 hours SM stress of type a and b scheme SM structure.

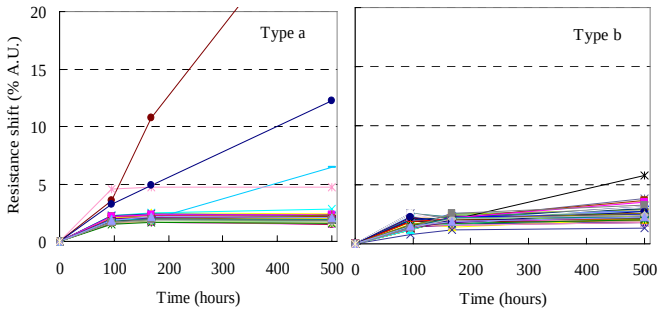

Fig. 3 Resistance change of via structures with time.

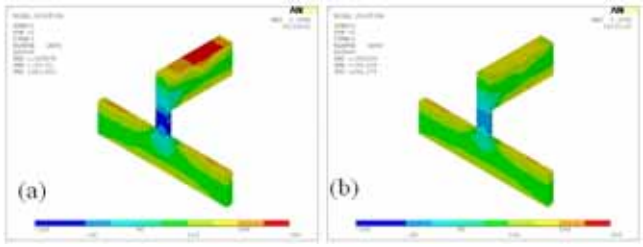

Fig. 4 Hydrostatic stress profiles in the via structure of type a and b scheme under 200C SM stress

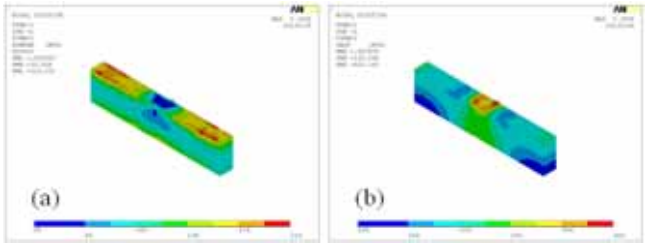

Fig. 5 (a) Hydrostatic and (b) von Mises stress profiles in bottom metal line of via structure under 200C SM stress.

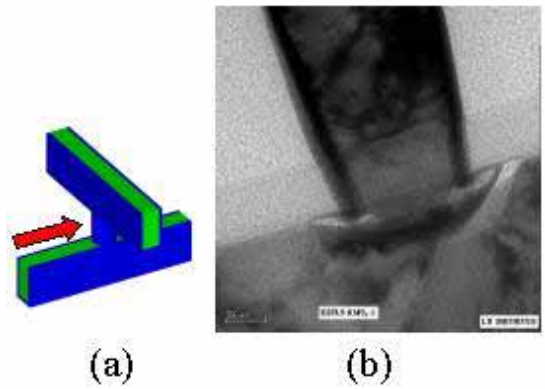

Fig. 6 (a) The TEM cross section direction in the SM structure. (b) The TEM picture shows metal void under the via bottom in the sample of scheme a structure with large resistance shift.

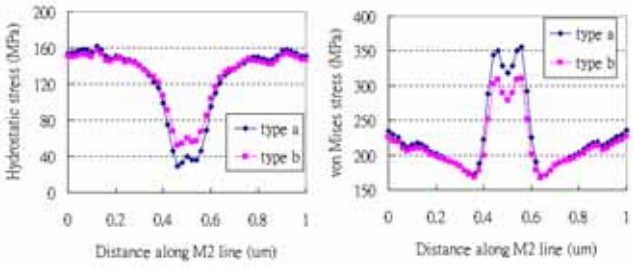

Fig. 7 Hydrostatic and von Mises stress along metal 2 surface.