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Analysis of threshold voltage variations of FinFETs : Separation of short channel effects and space charge effects

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1. Introduction

Double-gate MOSFETs, such as FinFETs, are promising device structures since they can suppress short channel effects (SCEs) essentially compared to the conventional planar MOSFETs [1-2]. As well as the SCEs, variation of device characteristics is an important issue in LSI technologies since it causes the trouble of the circuit performance [3], in which threshold voltage (*Vth*) variation is a significant problem [4].

In general, origins of the *Vth* variation of short channel devices are complicated and depending on device structures. We focus, in this paper, separation of factors related to the SCEs and the other ones independent of the SCEs. Based on the concept, the *Vth* variations of FinFETs are analyzed comparing to that of the conventional planar MOSFETs.

2. Simulation model

The FinFETs and the planar MOSFETs, as shown in Fig.1, were analyzed by using the Torus device simulator in 2D simulation mode, and common parameters used here are summarized in Table 1. The channel doping concentration (*Nc*) and fin width (*Wfin*) used in this work are summarized in Table 2. The conditions of planar MOSFEs and FinFETs referred to as No.II(A) in this table are close to those given in the ITRS2007 for generation of gate length (*Lg*) of 16 nm, where *Wfin*=(2/3)*Lg* for FinFETs. We added the conditions for FinFETs so that *Nc* identical to that of the planar MOSFETs and further aggressive narrowing of *Wfin* (*Wfin*=(1/3)*Lg*) were examined, according to the reports that *Wfin*<(2/3)*Lg* is necessary to suppress SCEs [5-6]. In addition, long channel devices (*Lg*=1.0 μm) having parameters identical to those of short channel devices, except for the *Lg*, were also simulated.

The variations of *Vth* were evaluated by *Vth* shift for 10% increase in *Lg*, *EOT* or *Nc*, and for 1.0 nm increase in *Wfin*. The deviation of *Wfin* was defined as an absolute value rather than the relative value considering realistic technical condition. The *Vth* variations were obtained for the short channel devices and long channel devices, and the differences in which the *Vth* for the long channel was subtracted from the *Vth* for the short channel were also calculated. The *Vth* variation for the long channel indicates the factor independent of SCEs, and the difference indicates the factor originated from SCEs.

3. Result and discussion

Figure 2 shows *Vth* variations for *Lg* deviation of +10%. For the short channel devices, those of FinFETs with the wider *Wfin* (=(2/3)*Lg*), I(A) and II(A), exhibited values larger than that of the planar MOSFET. The narrower *Wfin* (=(1/3)*Lg*), I(B) and II(B), suppressed the *Vth* shift effectively comparing to the planar MOSFET. For the *Lg* deviation, since no *Vth* variation was observed for the long channel, the *Vth* variation of the short channel devices are fully originated from SCEs.

The *Vth* variations for the EOT deviation are shown in Fig. 3. Although those for short channel devices exhibited positive value or negative value depending on the condition, rather large absolute values for FinFETs with low *Nc* condition are noted. However, it should be also noted that, typically for the planar MOSFETs, the large positive deviation of *Vth* for long channel, which is related to space charge in depletion layer, and the large negative deviation of the difference in *Vth*, which is related to SCEs, exist. The apparent small *Vth* variation for the planar MOSFETs is resulted from compensation between the two large deviation factors with opposite signs.

The *Vth* variations for the *Nc* deviation are shown in Fig. 4. Those for FinFETs, especially for the low *Nc* devices, II(A) and II(B), are smaller than that of the planar MOSFETs. The *Vth* variations for the short channel devices are determined by the space charge effect (relating to the long channel characteristics) mainly and are not affected by SCEs. The lower *Nc* is preferable to suppress the *Vth* variation since it becomes not significant for determination of *Vth*.

The *Vth* variations for the *Wfin* deviation (here, not +10% but +1.0 nm) on FinFETs are shown in Fig. 5. The compensation between the space charge effects and SCEs discussed above in the EOT deviation case (in Fig.3) plays an important role also in this case. The higher *Nc*, I(A) and I(B), suppress the apparent *Vth* variation by this mechanism, while the enhanced negative *Vth* variation appears for the lower *Nc*, II(A) and II(B). The negative variation for the long channel is explained by volume inversion and carrier depletion near the fin surfaces by the quantum confinement effect.

4. Conclusions

The *Vth* variations of FinFETs caused by various deviations of parameters of device structures were examined and summarized in Table 3. The apparent *Vth* variation includes different factors of space charge effects and SCEs, and the effects of compensation between these two factors reduce the apparent *Vth* variation in some cases. This view point is important to discuss the problem of *Vth* variation and will be necessary to design FinFETs robust for structural fluctuations.

Acknowledgements

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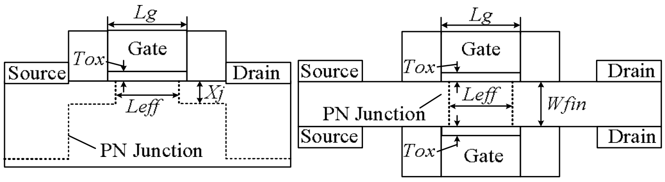

(a) (b)

Fig.1 Simulation models used in this work.
(a) conventional planar MOSFET and (b) FinFET.

Table 1 Size parameters commonly used in this work.

Gate Length (Lg)	16 nm (short channel)
Effective Gate Length (*Leff*)	12.5 nm
EOT (nm)	0.5nm (*Tox* = 2.7nm(HfO_2))
Junction depth (Xj)	5.8nm

Table 2 Varied parameters for FinFETs.

	Number	Channel doping concentration (*Nc*)	Fin width (*Wfin*)
Planar MOSFET		8.1×10^{18} cm^{-3}	-
FinFET	I (A)	8.1×10^{18} cm^{-3}	10.7 nm
	I (B)	8.1×10^{18} cm^{-3}	5.3 nm
	II (A)	1.0×10^{17} cm^{-3}	10.7 nm
	II (B)	1.0×10^{17} cm^{-3}	5.3 nm

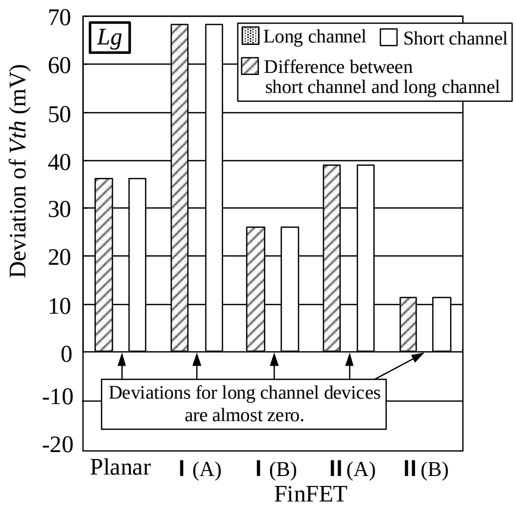

Fig.2 *Vth* variations for 10% increase in *Lg*.

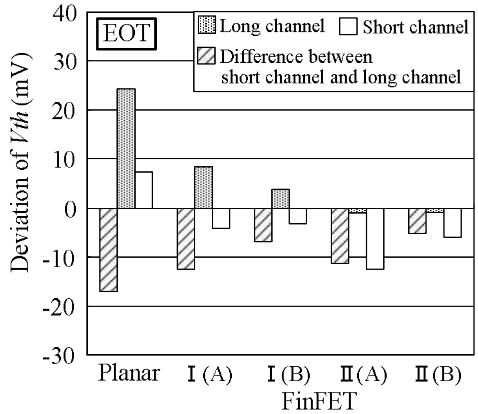

Fig.3 *Vth* variations for 10% increase in *EOT.*

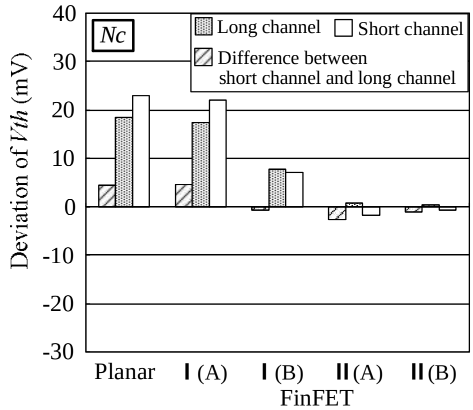

Fig.4 *Vth* variations for 10% increase in *Nc*.

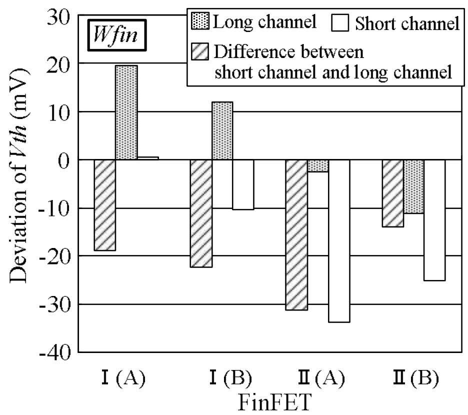

Fig.5 *Vth* variations for 1.0 nm increase in *Wfin.*

Table 3 Summary of *Vth* variations depending on parameters of device structure.

deviating parameter	superiority of FinFETs	narrow *Wfin* preferable	small *Nc* preferable
Lg	*	Yes	Yes
EOT	**	**	No
Nc	Yes	Yes	Yes
Wfin	--	**	No

* : depending on *Wfin* and *Nc*
**: depending on the compensation effect