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Extraction of Vertical, Lateral locations and Energies of Hot-Electrons-Induced Traps Through the Random Telegraph Noise

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Introduction

The influence of hot-carrier injection on the performance of MOS transistors has been studied during the last decade. The trap depth and energy were roughly extracted using trapping and de-trapping electrons of RTS noise after hot carrier stress [1-2]. In this paper, we extracted not only trap depth (x_T) and trap energy (E_{Cox}-E_T) but also lateral location (y_T) using accurate equations.

Experimental Data and Discusison

The deep-submicrometer MOSFET's used in this study were fabricated using a photoresist-ashing, dry etch, and plasma deposition in a 90 nm CMOS technology. The oxide thickness is 7 nm and substrate dopng density is 5×10^{16} cm^{-3}. The drain current fluctuations were measured by an 35670A spectrum analyzer at room temperature. Fig. 1 shows the typical current fluctuations of nMOSFET with L_{eff}=270 nm and 390 nm. No current fluctuation was founded before stressing as shown in the inset of Fig.1. Fig. 1(a) and (b) show the random telegraph noise after 10 min of channel hot electron stressing at V_g=2.75 V and V_d=5 V for device of L_{eff}=270 nm and 390 nm respectively. The trap depth was extracted by using eq.(1) [3-4].

$$x_T = \frac{T_{ox}\left(\frac{kT}{q}\frac{d\ln\frac{\tau_c}{\tau_e}}{dV_g}+\frac{d\psi_s}{dV_g}\right)}{\left(\frac{d\psi_p}{dV_g}+\frac{d\psi_s}{dV_g}-1\right)} \quad (1)$$

Here, T_{ox} is the oxide thickness and k is Boltzmann constant, τ_c and τ_e is capture and emission time. ψ_s is surface potential and ψ_p is poly depletion voltage drop. Through linear fitting process as shown in Fig. 2, $\ln(\tau_c/\tau_e)$ with respect to the gate voltage was obtained. The accurate vertical trap depths obtained by using eq.(1) are 5.8 nm and 2.9 nm for devices of L_{eff}=270 nm and 390 nm, respectively. Using information of vertical location of trap and ratio of τ_c/τ_e for forward bias and τ_c/τ_e for reverse bias of Fig. 3(a), lateral location of trap could be extracted with eq.(2) [3].

$$y_T = \frac{\frac{kT}{q}\frac{T_{ox}}{x_T}\ln\left[\frac{(\tau_c/\tau_e)_f}{(\tau_c/\tau_e)_r}\right]+V_{ds\,r}}{\frac{V_{ds\,r}+V_{ds\,f}}{L_{eff}}} \quad (2)$$

Fig. 3(b) shows the results which are 225 nm and 296 nm from source for device of L_{eff}=270 nm and L_{eff}=390 nm respectively. Also, the dfference between the oxide conduction band energy (E_{Cox}) and trap energy (E_T) could be extracted with eq.(3) [3-4].

$$\begin{aligned}(E_{Cox}-E_T) &= \phi_0 - q\psi_s + (E_C - E_{Fp} + q\frac{y}{L}V_{DS}) \\ &- q\frac{x_T}{T_{ox}}(V_g - V_{FB} - \psi_p - \psi_s) - k_B T\ln\frac{\tau_c}{\tau_e}\end{aligned} \quad (3)$$

Here, ϕ_0 is the difference between the electron affinities of Si and SiO_2, V_c si the channel potential at the point y in the channel measured from the source ($V_c \approx y_T V_{ds}/L_{eff}$), V_{FB} is flat band voltage. Using the known values of x_T and y_T, eq.(3) was evaluated and the result is shown in Fig. 4. Fig. 5 and 6 show the trap location in gate oxide and band diagram, respectively. Fig. 7(a) and (b) show the drain current fluctuation of another device before hot carrier stress and after hot carrier stress. From the same method explained above, physical parameters were obtained for device of L_{eff}=270 nm and L_{eff}=390 nm. From linear fitting results of Fig. 8, x_T for process-induced trap and stress-induced trap of device having L_{eff}=390 nm could be extracted. y_T could be also obtained for process-induced trap and stress-induced trap in Fig. 9(b). Also, using the x_T and y_T and eq.(3), energy level of the trap was extracted in Fig. 10. Fig.11 and 12 clearly shows trap locations in gate oxide and band diagram for process-induced trap and stress-induced trap, respectively. Table 1 lists the x_T, y_T, and E_{Cox}-E_T for process- and stress-induced traps. The hot carrier stress-induced traps are located in near drain region.

Conclusions

We measured the RTS noise after channel hot electron stressing. The depth of trap(x_T) and lateral location of trap(y_T) are obtained using accurate equations. We could confirm the hot-carrier stress induced traps are generated near the drain junction.

Acknowledgements

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Reference

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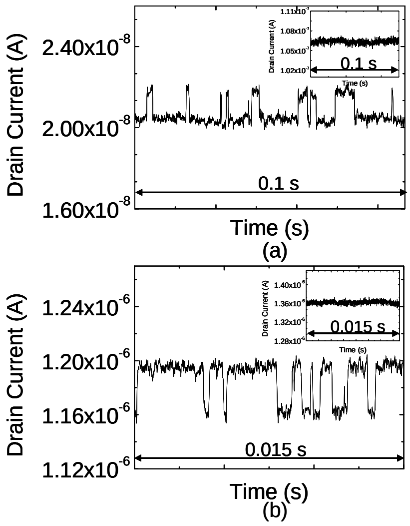

Fig. 1.RTS noise having two levels of (a) L_{eff}=270 nm and (b) L_{eff}=390 nm

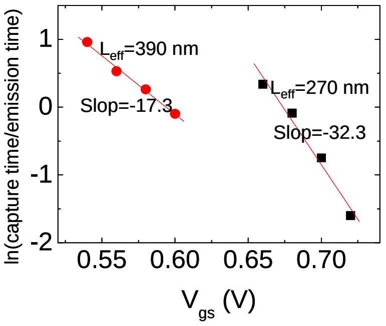

Fig. 2. ln(capture time/emission time) and its linear fitting.

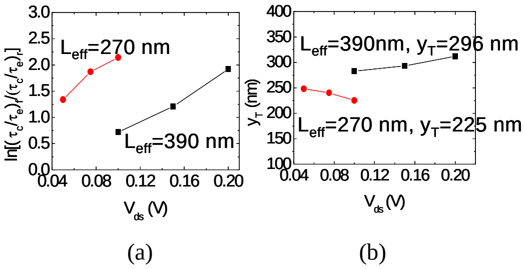

Fig. 3 (a) ln[(capture time/emission time) of forward bias/(capture time/emission time) of reverse bias] and (b) lateral position of traps by eq.(2).

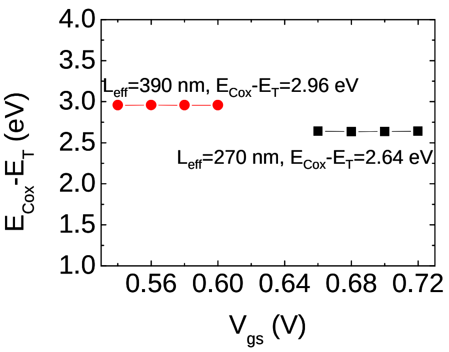

Fig. 4 E_{Cox}-E_T of traps calculated by eq.(3).

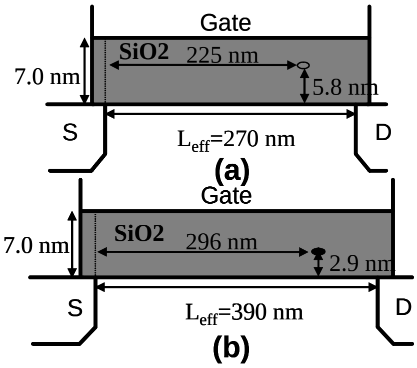

Fig. 5 Schematic of (a) trap location in gate oxide for L_{eff}=270 nm device and (b) for L_{eff}=390 nm device.

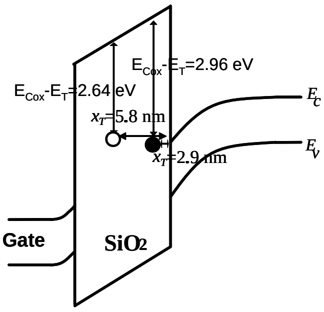

Fig. 6 Energy diagram of traps(white circle is L_{eff}=270 nm device and black circle is L_{eff}=390 nm device.

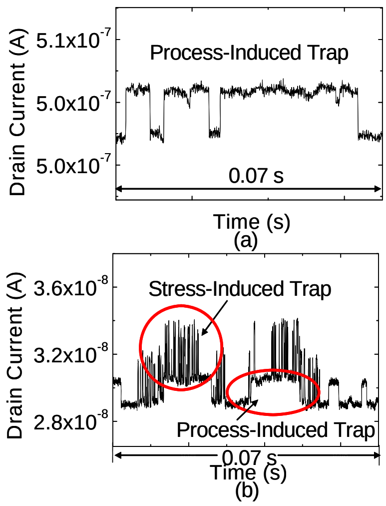

Fig. 7 RTS noise due to (a) process-induced trap and (b) stress-induced trap.

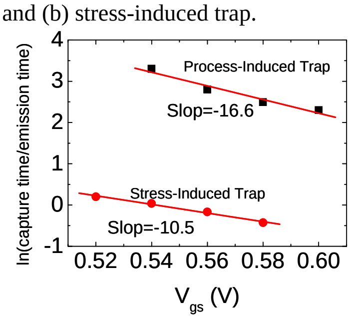

Fig. 8 ln(capture time/emission time) and its linear fitting for process-induced trap and stress-induced trap.

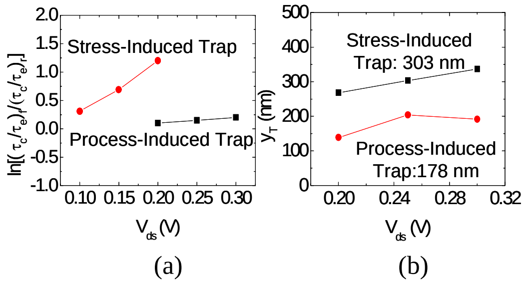

Fig. 9 (a) ln[(capture time/emission time) of forward bias/(capture time/emission time) of reverse bias] and (b) lateral position of traps by eq.(2).

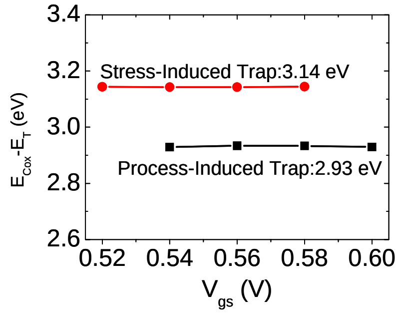

Fig. 10 E_{Cox}-E_T of traps calculated by eq.(3).

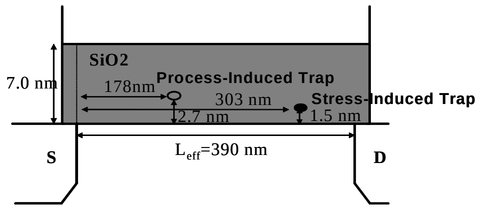

Fig. 11 Schematic of trap location in gate oxide of process-induced trap and stress-induced trap for L_{eff}=390 nm device.

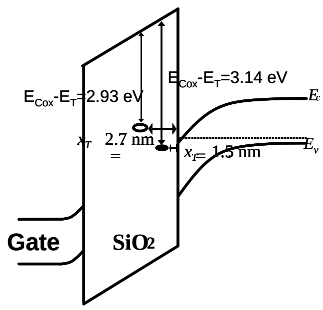

Fig. 12 Energy diagram of traps(white circle is process-induced trap and black circle is stress-induced trap.

Table 1. Lists of obtained x_T, y_T, and E_{Cox}-E_T.

L_{eff} (nm)	Pre-stress			Post-stess		
	x_T (nm)	y_T (nm)	E_{Cox}-E_T (eV)	x_T (nm)	y_T (nm)	E_{Cox}-E_T (eV)
270	-	-	-	5.8	225	2.64
270	6.7	184	2.50	2.2	209	3.01
390	-	-	-	2.9	296	2.96
390	2.7	178	2.93	1.5	303	3.14