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Hot-Carrier-Induced Degradation in p-type High-Voltage DEMOS Transistors

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1. Introduction

High-voltage devices such as Drain Extended MOS (DEMOS) or lateral DMOS (LDMOS) transistors are widely used in power applications. Since high-voltage device is operated under high V_{ds} and V_{gs}, hot-carrier reliability may become a serious concern. Recently, hot-carrier reliability of n-type DEMOS and LDMOS devices has been studied [1-3]. However, much less effort is done to address the reliability of p-type high-voltage transistors.

In this paper, hot-carrier reliability in p-type DEMOS devices is investigated. Charge pumping technique and TCAD simulations are performed to clarify the mechanisms of device degradation. Results show that the generation of interface state (ΔN_{it}) and negative oxide-trapped charge (ΔN_{ot}) are responsible for device degradation. ΔN_{ot} affects device characteristics at the beginning of stressing. ΔN_{it} dominates device degradation as the stress time is longer.

2. Experiments

Fig. 1 shows schematic cross section of the p-type DEMOS transistor used in this paper. This device is fabricated with a 0.35μm CMOS process. A lightly doped p-type region near the drain is designed as the drift region. The channel region, drift region under poly-gate, and drift region outside poly-gate are indicated as L, L_{ov}, and L_p, respectively. The operational voltage of the device is -15.3V for V_{ds} and -12V for V_{gs}. DC stressing under V_{ds}=-23V and various V_{gs} is performed at room temperature with the source and bulk tied to the ground. Linear drain current (I_{dlin}) is measured under V_{ds}=-0.1V and V_{gs}=-12V. Transconductance maximum (G_{mmax}) and threshold voltage (V_T) are extracted under V_{ds}=-0.1V. The stress tests are interrupted periodically to measure the shift of device parameters and charge pumping current (I_{cp}).

3. Results and Discussion

Fig. 2 shows I_g–V_{gs} and I_{sub}–V_{gs} characteristics of the device with L=1μm, L_{ov}=0.2μm, and L_p=1μm biased at V_{ds}=-23V. I_g peak occurs at V_{gs}=-3V, while two I_{sub} peaks are observed. The 1st I_{sub} peak occurs at V_{gs}=-4.1V and the 2nd peak occurs at V_{gs}=-12V. The 2nd I_{sub} peak is the result of Kirk effect [4]. In our experiment, the stress condition of V_{gs} that causes the most device degradation is V_{gs}=-12V. Small degradation (< 1%) is observed at I_g peak and 1st I_{sub} peak stress condition. Thus, we focus on V_{gs}=-12V stress condition in the following analysis. Fig. 3 shows the shift of device parameters under V_{ds}=-23V and V_{gs}=-12V stress. After stressing, $|V_T|$ is increased and G_{mmax} is degraded. However, $|I_{dlin}|$ is increased and shows turnaround behavior as the stress time is longer than 5000 s.

To identify the mechanism of device degradation, I_{cp} of the device in Fig. 3 is measured to evaluate ΔN_{it} and ΔN_{ot} in L and L_{ov} regions [5]. The experimental setup and I_{cp} results are shown in Figs. 4 and 5. The pulse train is applied to gate and bulk is grounded. In Fig. 4, the base level of gate pulse is fixed at -4V and varies the peak value of gate pulse from -4V to 1V. Drain is floating and source current is monitored as I_{cp}, which can evaluate ΔN_{it} and ΔN_{ot} in L region. In Fig. 5, the base level of gate pulse is fixed at 0V and varies the peak value of gate pulse from 0V to 12V. Source is floating and drain current is monitored as I_{cp}, which can evaluate ΔN_{it} and ΔN_{ot} in L_{ov} region. As the stress time increases, significant increase but no lateral shift in I_{cp} results (in Figs. 4 and 5) reveal that significant ΔN_{it} but small ΔN_{ot} is created in L and L_{ov} regions during stressing. Such a result suggests that the mechanism of V_T and G_{mmax} degradation is ΔN_{it} located in channel region.

Since ΔN_{it} created in L and L_{ov} regions can not explain $|I_{dlin}|$ increase after stress, TCAD simulations are performed to evaluate the damage created in L_p region. The impact ionization contour and current flow when V_{gs} is biased under I_g peak, 1st and 2nd I_{sub} peaks are shown in Fig. 6. Two observations are found. First, the impact ionization center at I_g peak and 1st I_{sub} peak condition is far beneath Si/SiO_2 interface. Device stressed under I_g peak and 1st I_{sub} peak condition results in small degradation because most of the current do no flow through the region where impact ionization rate is high. Second, another impact ionization center occurs near p^+ drain when V_{gs} is 2nd I_{sub} peak condition. Since significant current flows through the impact ionization center near p^+ drain, damage located in L_p region is expected. It is inferred that the impact ionization center near p^+ drain causes electron trapping in L_p region as the electric field at drain-side is favor for electron injection (V_{ds}=-23V, V_{gs}=-12V). Negative ΔN_{ot} increases surface hole concentration in L_p region, resulting in $|I_{dlin}|$ increase.

According to the above analysis, Fig. 7 illustrates the degradation mechanisms in our p-type DEMOS transistors. ΔN_{it} in channel region causes V_T and G_{mmax} degradation, while negative ΔN_{ot} in L_p region leads to $|I_{dlin}|$ increase. Fig. 8 shows $|I_{dlin}|$ shift of devices with various lengths in L and L_p. Results show that $|I_{dlin}|$ increases at the beginning but $|I_{dlin}|$ shift is turnaround after roughly 5000 s. Such a result suggests that ΔN_{it} in L and L_{ov} regions dominate the device degradation as the stress time is longer [6].

4. Conclusions

Hot-carrier-induced degradation in p-type DEMOS devices is discussed. The V_{gs} biased at 2nd I_{sub} peak produces the most degradation. The mechanisms of device degradation are ΔN_{it} in L and L_{ov} regions, as well as negative ΔN_{ot} in L_p region. As the stress time is longer, ΔN_{it} in L and L_{ov} regions dominates device degradation.

Acknowledgements

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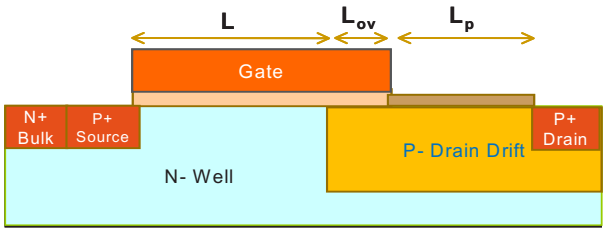

Fig. 1 Cross section of p-type DEMOS device used in this paper.

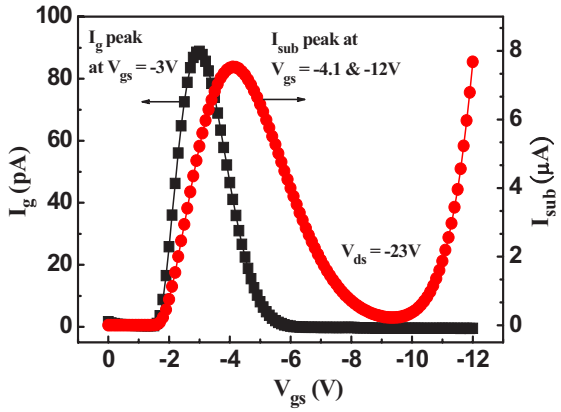

Fig. 2 I_g–V_{gs} and I_{sub}–V_{gs} characteristics of p-type DEMOS device. I_g, 1st, and 2nd I_{sub} peaks occur at V_{gs} = -3V, -4.1V, and -12V.

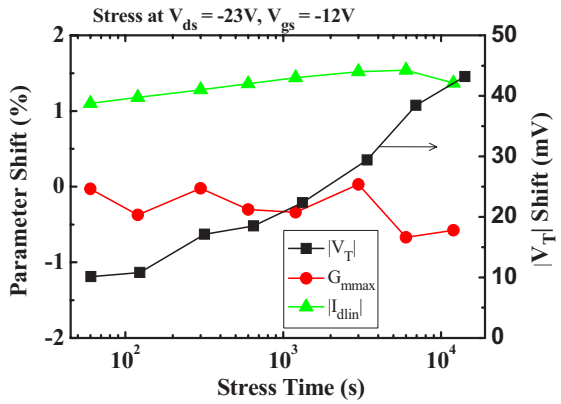

Fig. 3 Device parameter shift during hot-carrier stress. $|V_T|$ and G_{mmax} are degraded. $|I_{dlin}|$ is increased.

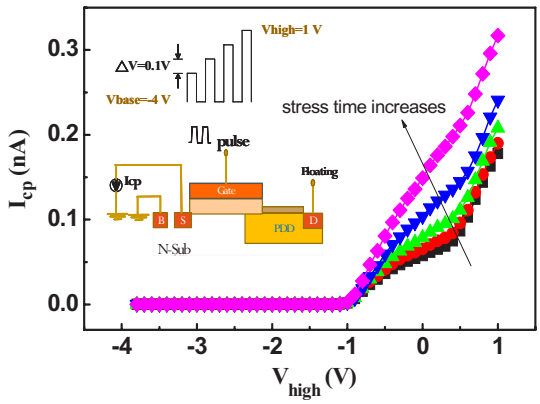

Fig. 4 I_{cp} resulted from damage located in L region. Significant ΔN_{it} but small ΔN_{ot} is created.

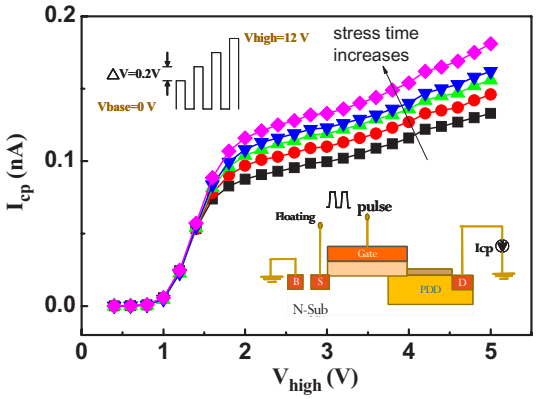

Fig. 5 I_{cp} resulted from damage located in L_{ov} region. Significant ΔN_{it} but small ΔN_{ot} is created.

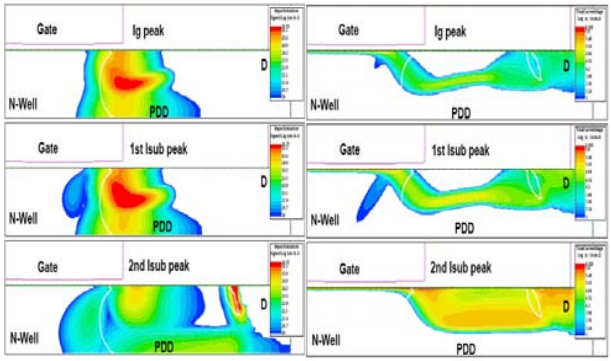

Fig. 6 Impact ionization (left) and current flow (right) when V_{gs} are biased under I_g peak, 1st, and 2nd I_{sub} peak conditions.

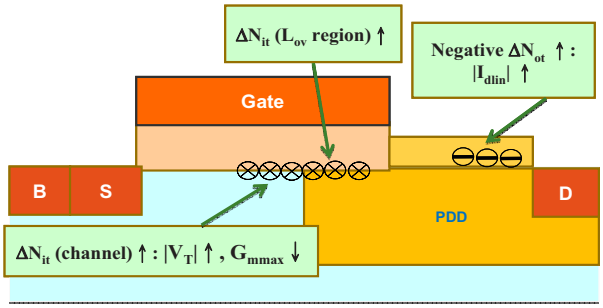

Fig. 7 Proposed two mechanisms for device degradation. ΔN_{it} in channel region results in V_T and G_{mmax} degradation. Negative ΔN_{ot} in L_p region results in $|I_{dlin}|$ increase.

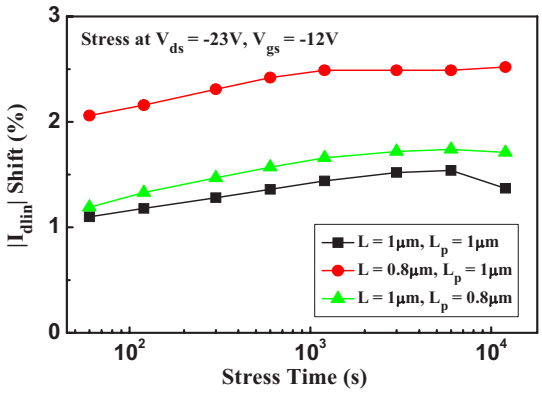

Fig. 8 Turnaround in $|I_{dlin}|$ shift suggests that ΔN_{it} in L and L_{ov} regions dominate device degradation as the stress time is longer.