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Modeling of Substrate Current of MOSFETs under Different Gate Biases and Temperatures

S. Y. Chen[1,*], C. H. Tu[1], M. C. Wang[1,2], S. H. Wu[3], Z. W. Jhou[3], C. J. Chang[3], J. Ko[3], and H. S. Huang[1]

[1]Institute of Mechatronic Engineering, National Taipei University of Technology
1, Sec. 3, Chung-Hsiao E. Rd., Taipei 106, Taiwan
*Email: sychen@ntut.edu.tw, Tel: 886-2-27712171 ext. 2011, Fax: 886-2-27717318
[2]Department and Institute of Electronic Engineering, Minghsin University of Science and Technology
[3] Integration Technology Division, United Microelectronics Corporation

Abstract—In this work, the problem of substrate current exhibiting different temperature dependences at different drain voltages is investigated. The unsolved so-call "transition point" is cleared up and a new mathematical model for substrate current is proposed. With the evidence from experiments, this paper points out that using the substrate current to monitor the severity of hot-carrier (HC) effect is lost its accuracy.

1. Introduction

Many of current and future generations of CMOS integrated circuits are inevitably to be operated at high temperature. State-of-the-art microprocessors reportedly have an average power density of over 100 W/cm^2 and the junction temperature often exceeds 100 ℃ [1-2]. Therefore, temperature effect has become a critical factor affecting device performance and reliability.

As CMOS devices continuously shrinking, related studies showed that the impact ionization had a transition point (voltage), which reversed the dependence of a MOSFET's substrate current (I_b) on temperature [3-4]. This finding was proved with the result in which the peak I_b would reverse its temperature dependence when the drain voltage (V_d) was biased across the transition point. This anomalous phenomenon renders the necessity of remodeling the I_b taking account of gate biases and temperatures. It also sparks another debate about the correction of I_b with MOSFETs' hot-carrier (HC) degradation. In short, can I_b still be applicable to monitoring the HC effects? These combine with the behind mechanisms still remain unclear even to the present.

2. Problem of transition point

To clearly understand the problem of transition point, the source current (I_s) reduction due to phonon scattering at high temperature needs to take a closer look. Figure 1 illustrates I_s of the nMOSFETs versus V_g at V_d = 3.2 V. The samples are the I/O devices of 0.13 μm technology having 120 nm gate length and 32 Å gate oxide thickness. Note that high temperature has lowered I_s due to the phonon scattering as the inherent mobility degraded proportional to $T^{-1.5}$ where T is absolute temperature in degree K [5], also the ratios of I_s between different temperatures at V_d = 2.8 V or 2.4 V were found to be about the same of V_d = 3.2 V. For pMOSFETs, similar results were also obtained at V_d = -2.8, -3.4, -3.6 V.

Tables 1 provides the explanation of the transition point for nMOSFETs where I_{b0} is the substrate current at V_g= 0 V. To unveil the mystery of transition point, it can be concluded that temperature does not generate different I_{bm} dependences alone as in Figure 2. On the contrary, higher temperature always provides additional thermal (kinetic) energy and results in higher impact ionization rate although the effect is narrowed down at high drain voltage. This can be observed from the fourth column of Table 1. The narrowed effect combining with the I_s reduction due to phonon scattering at high temperature constitute the phenomena of transition point. To conclude this section, it is clear to say that if V_d is lower than the transition point, then the effect of phonon scattering induced I_s lowering is smaller than the effect of elevated temperature provided thermal energy such that the I_{bm} will occur at high temperature.

3. Modeling of the substrate current

The substrate current (I_b) is long being taken as the indicator of the severity of HC effects, especially for the nMOSFETs on the drain avalanche HC stress mode. Additionally I_b always exists in the normal operation of MOSFETs and forms a part of current leakage. Therefore it is important to model I_b properly.

It is well known that I_b comes mainly from the impact ionization at velocity saturation region. Previous researches, either using lucky electron model [6] or more complicatedly using impact ionization rate to integrate [7], focused mostly on the influences of lateral electrical field and seldom considered the temperature effects as well as the transverse electrical field, i.e. the influence of gate biases. Therefore, it is found that they can not adequately present the data of this work within acceptable accuracy.

To improve the accuracy of the modeling and to include the influences of temperature and transverse electrical field in most simple form, a new substrate model for nMOSFETs is provided as

$$I_b = I_s \exp(AE_{eff} + BE_{av} + CT + D) + I_{b0} \quad (1)$$

where E_{eff} is the transverse electrical field at the middle of inversion layer; E_{av} is the average lateral electrical field along the velocity saturation region; T is the absolute temperature in degree K; A, B, C and D are fitting constants.

Figures 3 to 5 compare the measured results to the calculated results from Eq. (1). Although considerable errors exit in the above comparisons, however for calculating I_b at lower V_g region and near I_{bm}, the errors are still acceptable. After all, using only four fitting constants to express the effects of transverse field, lateral field, and temperature, Eq. (1) is the first one.

4. HC induced degradation issue

Many HC stress tests were performed on the previous mentioned MOSFETs. In the case of the stressed drain bias set lower than the transition voltage, Figure 6 shows no reverse temperature effect at Vd = 2.2 V after HC stress. Note that this is in contradiction to a higher temperature possessing a higher Ibm as shown in the Figure 2 because room temperature still reveals the largest degradation among different temperatures for three types of drain currents. Actually, for drain bias set at the transition voltage, i.e., Vd = 2.8 V, the results are the same as above. In addition, pMOSFETs were also tested and reveal about the same results.

5. Conclusions

The most significant findings in above studies can be described as the following. The mystery of the transition point about the different temperature dependences of substrate current is solved, both for n and pMOSFETs. To include the influences of temperature and transverse electrical field, a new substrate model for nMOSFETs is provided. It is also found that using Ibm to monitoring the HC effects is

only suitable for drain voltages larger than transition voltages of the MOSFETs, but for Vd smaller than the voltages it is not safe to do so.

References

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Table 1. Data for the explanation of maximal substrate currents of nMOSFETs.

V_d (V)	Temp. (℃)	I_s (A)	$(I_b$-$I_{b0})/I_s$	I_{bm} (μA)
2.4	125	-0.00744	0.00604	44.95
	25	-0.00871	0.00486	42.35
Ratio	125 data/25 data	0.85392	1.24305	1.06
2.8	125	-0.00876	0.02054	179.93
	25	-0.01009	0.01783	179.99
Ratio	125 data/25 data	0.86801	1.15168	1.00
3.2	125	-0.01007	0.05716	575.84
	25	-0.01128	0.05264	594.03
Ratio	125 data/25 data	0.89275	1.08584	0.97

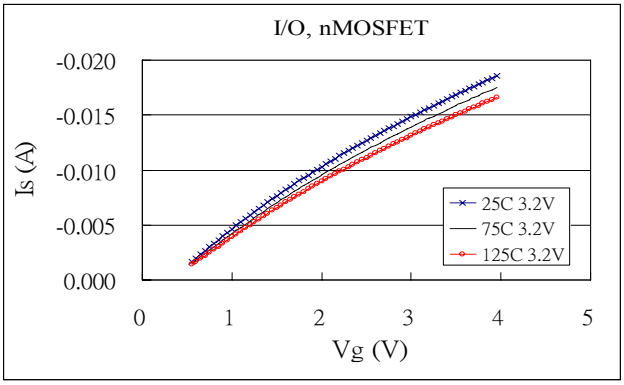

Fig. 1. Source currents of nMOSFETs versus V_g at V_d = 3.2 V.

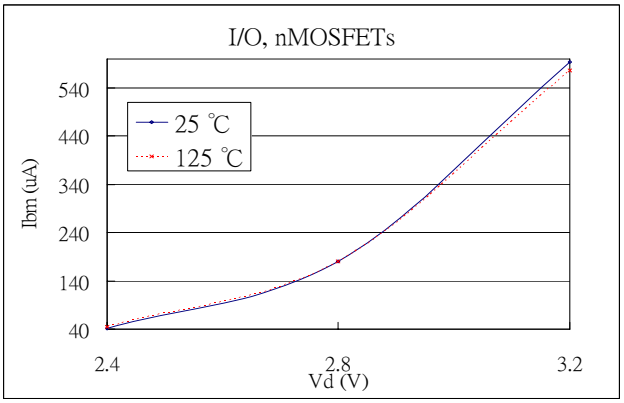

Fig. 2. Maximal substrate currents versus drain voltages. Note that the transition point is found at 2.8 V.

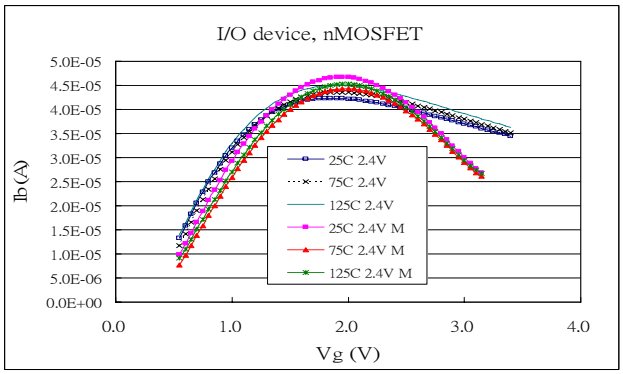

Fig. 3. Comparison of measurements with calculations from obtained model, as indicated "M", at V_d = 2.4 V.

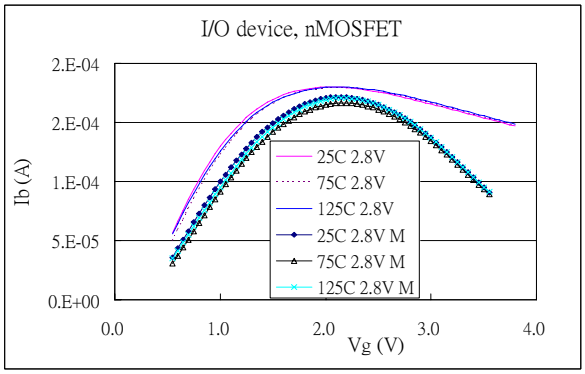

Fig. 4. Comparison of measurements with calculations from obtained model, as indicated "M", at V_d = 2.8 V.

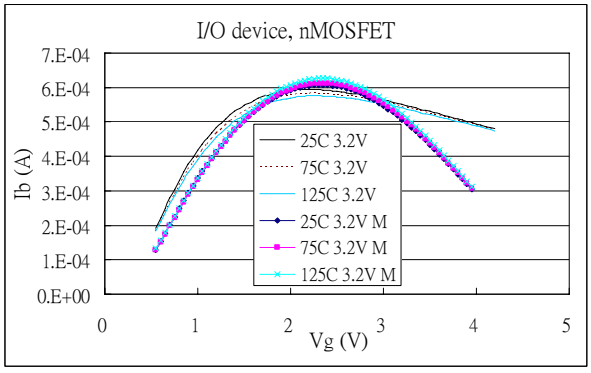

Fig. 5. Comparison of measurements with calculations from obtained model, as indicated "M", at V_d = 3.2 V.

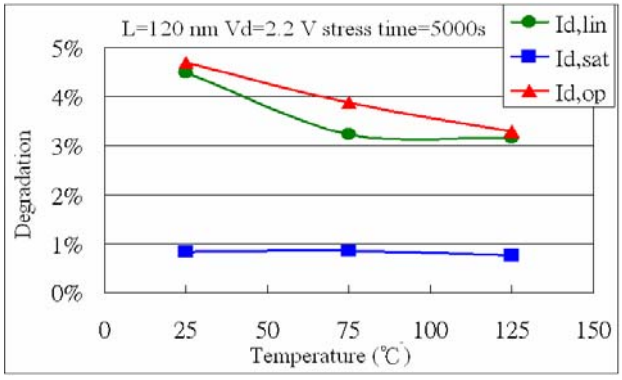

Fig. 6. Drain current degradation on nMOSFETs versus temperatures at V_d = 2.2 V after stress for 5000 s on DAHC stress mode. $I_{d,op}$ is the drain current measured at analog operation condition.