Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 434-435

P-3-16

Optimization of Source/Drain Overlap to Gate for 16 nm Gate Last MOSFETs

Junyong Jang, Towoo Lim, Hyungtak Kim and Youngmin Kim

School of Electrical Engineering, Hong Ik University
72-1 Sangsu-Dong, Mapo-Gu, Seoul, 121-791, Korea
Phone: +82-2-320-3097 E-mail: jjy8112@gmail.com

1. Introduction

Recently, a gate last MOSFET is suggested as 32 nm node CMOSFET to overcome thermal stability, workfunction mismatch issues [1]. Also, the gate last process can considerably enhance carrier mobility obtained from embedded SiGe source/drain [2], but this approach likely suffers from a high overlap capacitance due to a high-k spacer sidewall. For better understanding of the performance impact, a comprehensive study on the gate last structure is needed. In this work, we investigate the effect of source/drain overlap to gate (gate/SDE) on performance of 16 nm gate last MOSFET using TCAD simulation.

2. Simulation methodology

A two-dimensional simulation tool (ATLAS) is used to design 16 nm CMOSFETs. The modified drift-diffusion model, BTBT model and QM model are employed for the nano-scale MOSFET simulation [3]. Fig.1 shows schematic cross-sections of the gate structures being considered in this work. All three types of the gate structures are recently reported [1-2] and can be fabricated by replacing a polysilicon gate with high-k/metal gate electrode after S/D anneal. Performance of such gate last MOSFETs are compared as a function of a S/D overlap. The physical channel length (distance between S/D extension) is 16 nm and equivalent oxide thickness (EOT) of the gate dielectric is 1 nm (including 0.5 nm interfacial layer). For structure 3 (high-k S/W MOSFET), high-k sidewall thickness ($L_{s/w}$) is assumed to be same with the EOT of the gate dielectric, considering a high-k deposition after removal of the polysilicon and the gate dielectric. Details of the MOSFET are assumed as suggested in 32 nm node ITRS [4]. Doping concentrations for channel, S/D extension, deep S/D are 5×10^{18} cm^{-3}, 5.5×10^{19} cm^{-3} and 2×10^{20} cm^{-3}, respectively. A metal gate of band edge work function is used for n/pMOSFET and S/D extension lateral abruptness is assumed to be 1.5 nm/decade.

3. Results and Discussion

I_{on} and C_{gate} for nMOSFET are simulated as a function of gate/SDE overlap length (L_{ov}) for the gate structures (Fig. 2). The I_{on} reduces for all three cases as the overlap decreases due to increased series resistance. However, structure 2 and 3 exhibit higher I_{on} for underlap cases. Fig. 3 shows profiles of electron concentration along the channel for a MOSFET with L_{ov} = -2 nm. More electrons are accumulated at the source region for the structure 2/3 due to higher vertical electric field, which is able to reduce the series resistance despite poor gate coupling of the underlap structure. Taking such resistance and capacitance into account, a mixed-mode simulation for a two-stage CMOS ring oscillator is carried out. The width ratio of nMOSFET and pMOSFET is chosen to be 1:2. The switching delay is simulated as a function of the overlap length (Fig. 4). Each gate structure shows the minimum delay at different L_{ov} values. The optimum overlap length for the conventional MOSFET is 1 nm, which agrees well with Taur's work [5]. But the minimum delay for the high-k S/W MOSFET (structure 3) is obtained at the underlap = 1 nm. Structure 2 exhibits less sensitivity to gate CD variation than the other structures. Fig. 5 illustrates delay time dependence on the permittivity of the gate dielectric layer in the high-k S/W MOSFETs. Optimum S/D design shifts toward the underlap structure as the permittivity of the gate dielectric layer increases, indicating the delay is dominated by the capacitance instead of the I_{on}. The subthreshold slope for the different structures is shown in Fig. 6. Fig 7 illustrates threshold voltage (V_{th}) and I_{off} current for the different gate structures when low standby power (LSTP) application is considered. In the regime of a low leakage current (I_{off} = 100 pA/um), I_{off} is determined by GIDL current which agrees with previously published work [6] (Fig. 8). The GIDL current is found to be affected by the gate/SDE overlap for structure 1/3, but structure 2 is not. Fig. 9 shows the electric field distribution for the S/D overlap and underlap structures. For the overlap case, the maximum electric field can be located away from the junction, leading to reduction of the GIDL current.

4. Conclusions

An optimized S/D design is suggested for the gate last 16 nm MOSFET. The high-k S/W MOSFET is found to be able to reduce a series resistance at the expense of a high parasitic capacitance. Contrary to the conventional MOSFET, an underlap S/D design is preferred for the high-k S/W MOSFET to minimize the delay time.

Acknowledgements

This work was supported by the Seoul R&BD Program (10555).

References

[1] Mistry. K., et. al., IEDM Tech. Dig., (2007) P.247~250.
[2] Mayuzumi, S., et. al., IEDM Tech. Dig., (2007) P. 293~296.
[3] J.D. Bude, SISPAD 2000, (2000) P. 23~26.
[4] ITRS 2006 Update.
[5] Minjian Liu, et. al., IEEE Trans. Elec. Dev., (2006) P. 3146~9.
[6] Lim, T., et. al., Electronics Lett., (2008) P. 157~158.

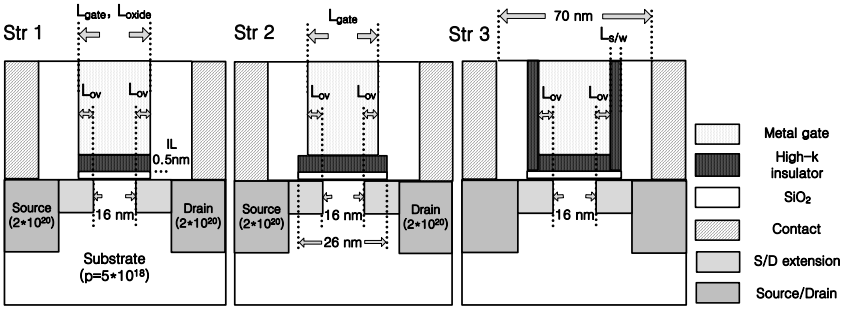

Fig.1 Schematic cross-sections of various gate structures. Structure 1 is conventional gate structure, which can be built by replacing polysilicon gate with metal gate. For structure 3, both polysilicon and gate dielectric are replaced by high-k/metal electrode, leading to high-k S/W MOSFET.

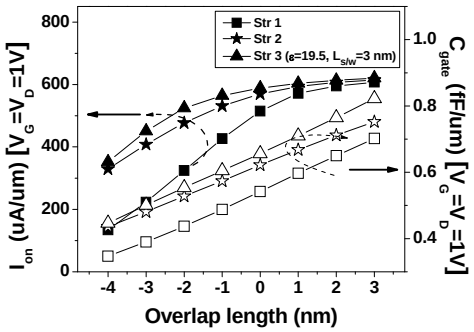

Fig.2 On-current and gate capacitance of nMOSFETs versus overlap length for various gate structures. For underlap cases, structure 2/3 show higher I_{on}, but also suffer from higher capacitance.

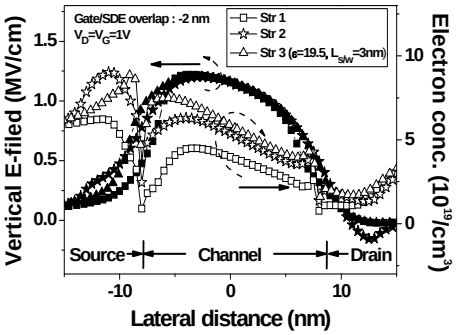

Fig.3 Profile of electron concentration at the surface of substrate for nMOSFET. More electrons are accumulated at the source region for structure 2/3 due to high vertical electric field.

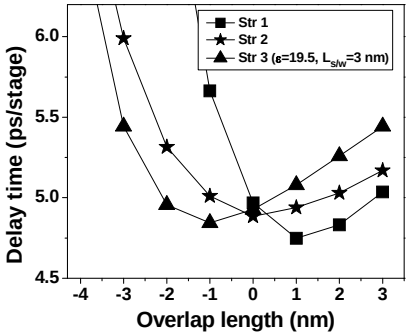

Fig.4 Delay time as a function of the overlap length (L_{ov}). Each gate structure shows the minimum delay times at different L_{ov} value.

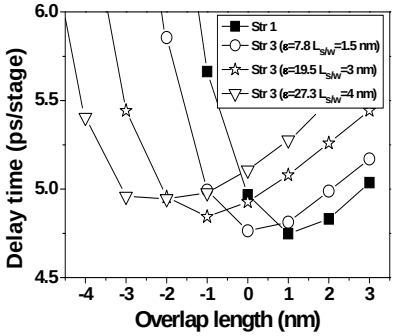

Fig.5 Delay time dependence on permittivity of gate dielectric layer in the structure 3. To meet same equivalent T_{ox}, the physical thickness is adjusted.

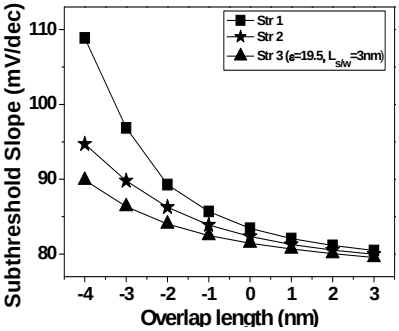

Fig.6 Subthreshold slope as a function of the overlap length. Better electrostatic control is achieved with high-k S/W MOSFET.

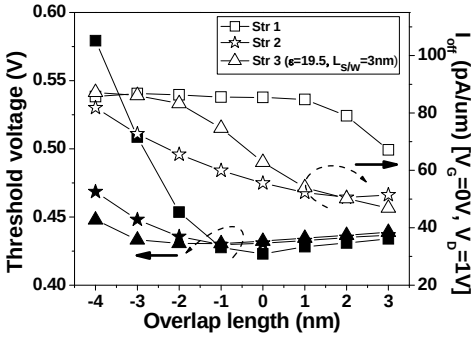

Fig.7 V_{th} and I_{off} versus overlap length for different gate structures. Lower leakages can be obtained in structure 2 and 3 due to better electrostatic control.

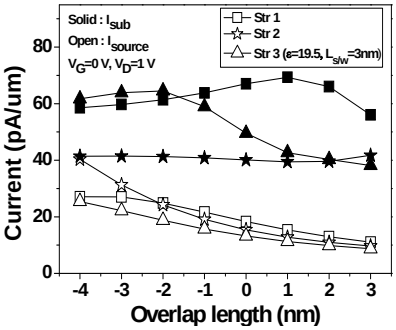

Fig.8 Subthreshold leakage and GIDL current versus overlap length. The leakage current is dominated by GIDL current instead of subthreshold leakage and affected by S/D overlap.

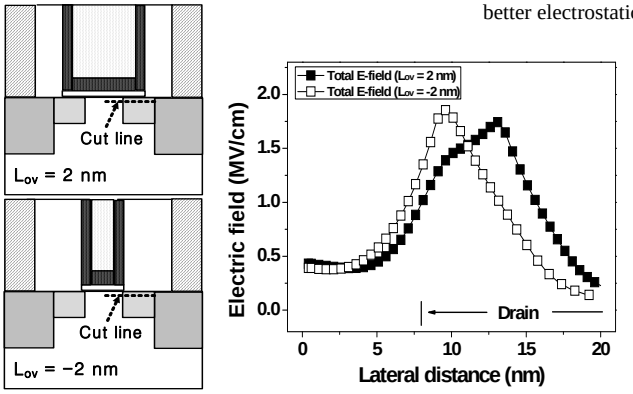

Fig.9 Electric fields for 2 nm S/D overlap and underlap structures. Maximum electric field can be located away from junction, leading to suppression of GIDL current.