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Effect of Nickel Silicide Intrusion on Schottky Barrier Nanowire MOSFET Fabricated Using Top-down Technology

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1. INTRODUCTION

The continued scaling of source/drain (S/D) junction depth in conventional MOSFETs results in several limiting factors including increased sheet resistance (R_{sh}) and limitations in doping/activation techniques to achieve sharp lateral doping profiles [1,2]. Schottky barrier MOSFET (SBMOS) architecture in which the metallic S/D regions are in direct contact with the transistor channel can essentially eliminate the S/D parasitic resistance and provide abrupt junction interfaces [3]-[5]. Recently, the effect of gate modulation on Schottky barrier thickness at source/drain has been shown to increase tunneling current [6,7]. However, this effect is significant when the silicide intrudes into the channel overlaps the gate [8], but controlling the distance of silicide intrusion in nanowire proves to be more challenging than in a 2-D planar transistor [9,10].

While work on silicide intrusion on bottom-up nanowire device have been investigated [9], nickel silicide intrusion and its impact on Schottky transistor's performance on top-down nanowire transistor by method of lithography are reported in this work. For the first time, we demonstrate that controllable silicide intrusion of less than 40 nm can be realized by using different RTA conditions in top-down nanowire transistor.

2. EXPERIMENTAL

Fig. 1 shows the integration scheme of the nickel silicided S/D Schottky omega-gate nanowire transistor. Si fins were patterned on p-type ($1x10^{15}cm^{-3}$) SOI wafers, followed by oxidation at 1050 ^{o}C to grow 500 Å oxide. The oxide was then thinned down to 300-350 Å as gate dielectric before polysilicon deposition as the gate. Both thin body with W=1µm and nanowire transistors were fabricated on the same wafer. **Fig. 2** shows the cross sectional TEM which confirms the omega shape gate and shows the silicon nanowires formed were about 30 nm in diameter. After gate etch and S/D pad oxide removal, the S/D Si thickness was about 30 nm prior to Ni deposition. A proposed 2-step RTA silicidation schemes are shown in **Table I**. A 1-step RTA silicidation was used as a control, as indicated as Split no. 5.

3. RESULTS AND DISCUSSION

Fig. 3 TEM shows TEM/EDX analysis on different locations near the silicon/silicide interface below the gate of a thin body transistor. The Ni to Si ratio shows the silicide formed at 275 ^{o}C was Ni-rich silicide and the 30 nm-thick source/drain was fully silicided by annealing 30 nm Ni for 30 s. It has been observed that the Ni to Si ratio gradually decreases from the S/D to the silicon/silicide interface.

Fig. 4 shows the transfer characteristic (I_D-V_G) for SB (Schottky Barrier) nanowire and thin body transistor with a gate length = 350 nm. The nanowire transistor shows superior sub-threshold slope and higher drive current than that of the thin body device due to better electrostatic coupling from the omega shape gate.

Fig. 5 shows the sub-threshold slopes of the SB nanowire transistor at different gate lengths with various silicidation conditions at low RTA temperature of 275 ^{o}C. It is clear that silicidation with Ni thickness of 14 nm, the sub-threshold performance is poor and has larger scattering compared to the Ni thickness of 30 nm. At 275 ^{o}C, it is believed that Ni-rich silicide phase was formed and due to the limited supply of Ni, the thinner Ni film would be insufficient to fully silicide the S/D. Hence, worse sub-threshold slopes and higher leakage current were observed for the 14 nm-Ni devices. We also found that with 14 nm Ni, the 30 s annealing shows better sub-threshold slopes than that of 60 s.

Fig. 6 shows the improvement in the short channel performance of the SB nanowire transistor after a 2nd RTA. The 14nm-Ni devices annealed with 1st RTA at 275 ^{o}C, 60 s shows significant improvement in the sub-threshold slope, whereas the 30nm-Ni devices show only minimal improvement. **Figs. 7** and **8** show the transfer curves for a 350 nm gate SB nanowire transistor before and after 2nd RTA at 450 ^{o}C silicided with the 14 nm Ni. The sub-threshold slope significantly improved from ~300 mV/dec to 130 mV/dec. However, there is no considerable change in the drive current of the device, suggesting that the Schottky barrier height remained unchanged before and after the 2nd RTA.

Fig. 9 shows the I_D-V_G of two 750 nm gate length nanowire transistors, one with 1-step 450 ^{o}C, 30 s with 14 nm Ni and another with 2-step RTA with 1st RTA at 275 ^{o}C, 60 s with 14 nm Ni, followed by the 2nd RTA at 450 ^{o}C, 30 s after removal of the unreacted Ni. The sub-threshold regions for the two devices are almost identical, but the drive current for the 1-step RTA device is higher than that of the 2-step RTA. **Fig. 10** shows the intrusion of nickel silicide into the nanowire channel of nanowire transistors with three silicidation splits. Fig. 10(a) and (b) show that after the 1st RTA at 275 ^{o}C for 30 s with Ni thickness of 14 and 30 nm, the lateral silicide intrusions are approximately 30 and 40 nm respectively. However in Fig. 10(c), the silicidation at 450 ^{o}C, 30 s with the 14 nm Ni shows severe intrusion of approximately 170 nm into the nanowire channel. This is consistent with the result that 1-step RTA device has a higher drive current than the 2-step RTA device as its effective channel length is much smaller than the physical gate length. However, excessive intrusion is undesirable as it increases the parasitic capacitance, hence increasing the RC delay of the device and degrading its speed.

4. CONCLUSION

Nickel silicide intrusion in silicon nanowire is presented. It has been shown that by using a 2-step RTA, intrusion can be well controlled by forming nickel rich silicide at lower temperature and then etching back excess Ni. A 2nd RTA can improve the transistor performance. By designing the spacer thickness carefully, intrusion with minimal overlap with gate can be fabricated.

References: [1] Y. Taur *et. al* , *IEDM*, p 789, 1998. [2] Y, Taur *et. al*, *Cambridge University Press*, Cambridge, 1998. [3] A. Kaneko *et. al*, *IEDM*, p 893, 2006. [4] Q. T. Zhao *et. al*, *Proc. IWJT*, p 147, 2006,. [5] A. Kinoshita *et. al*, *VLSI*, p 168, 2004. [6] Indlekofer *et. al*, *TED*, p 1502, 2007. [7] Appenzeller *et. al*, *PRL*, p 48301, 2004. [8] Zhang, *ESSDERC*, p 457, 2005. [9] Appenzeller *et. al*, *IEDM*, 2006. [10] Seger *et. al*, *APL*, p 253507, 2005.

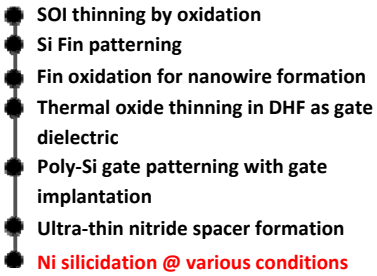

Fig. 1 Integration scheme of Schottky Si nanowire transistor with Ni silicided source/drain.

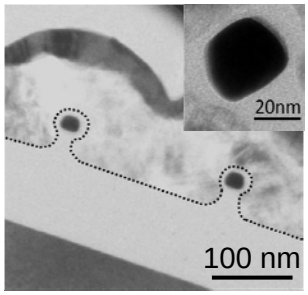

Fig. 2 X-TEM view of a twin nanowire omega-shape gate Schottky barrier transistor. The dotted lines indicate poly-Si/oxide interface. The inset shows Si nanowire with diameter approx. 30nm.

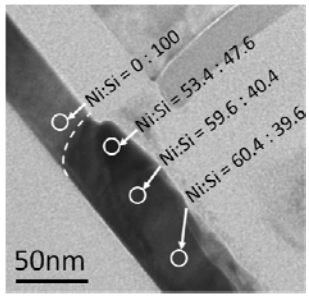

Fig. 3 TEM/EDX analysis near the drain silicide/silicon interface showing Ni-rich silicide is formed after RTA at 275°C for 30s with 30nm Ni. The dotted lines are guide to eyes for silicide/silicon interface.

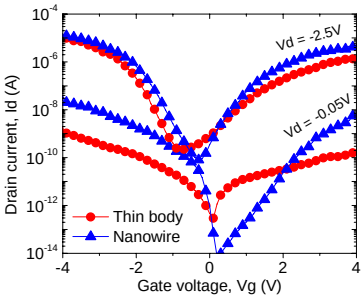

Fig. 4 I_D-V_G of nanowire and thin body devices with Ni silicide source/drain transistors annealed at 275°C for 30s with 30nm Ni.

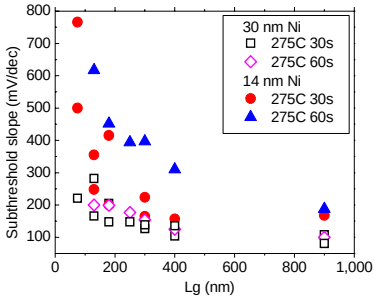

Fig. 5 Subthreshold slope vs. gate lengths for SB nanowire devices annealed at various Ni thickness and 1st RTA conditions.

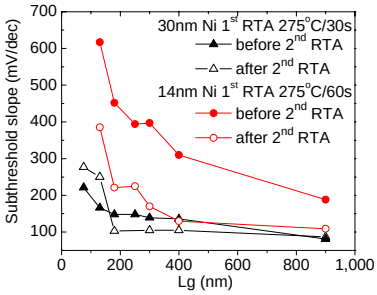

Fig. 6 Subthreshold slope vs. gate lengths for SB nanowire devices after 1st RTA with 14nm and 30nm Ni, followed by 2nd RTA at 450°C for 30s after etching back of excess Ni.

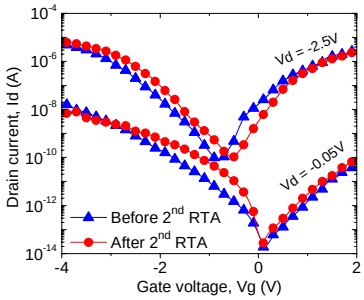

Fig. 7 I_D-V_G of SB nanowire transistors with 1st RTA of 275°C for 60s with Ni thickness of 14nm and a 2nd RTA of 450°C for 30s after etch back of excess Ni.

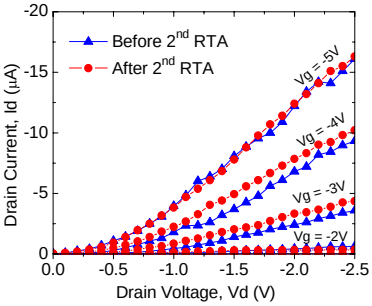

Fig. 8 I_D-V_D of SB nanowire transistors with 1st RTA of 275°C for 60s with Ni thickness of 14nm and a 2nd RTA of 450°C for 30s after etch back of excess Ni.

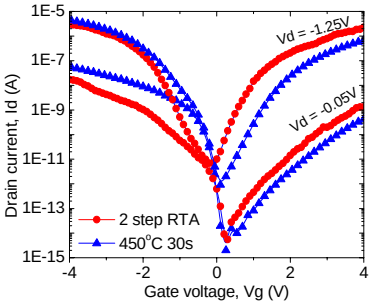

Fig. 9 I_D-V_G of SB nanowire transistors with 2 step RTA vs. 450°C 30s anneal.

Split	Ni Thickness (nm)	1st RTA 275 °C		Unreacted Ni removal after 1st RTA	2nd RTA 450 °C 30 s
		30 s	60 s		
1	14	●		●	●
2	14		●	●	●
3	30	●		●	●
4	30		●	●	●
5	14				●

Table I: Summary of different silicidation splits used for fabricating the SB nanowire transistors.

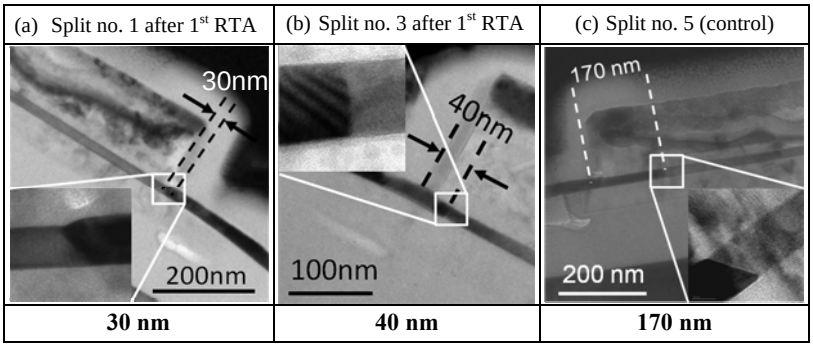

Fig. 10 TEM micrographs showing lateral intrusions of silicide into nanowire channels after annealed at various splits. The split numbers are shown above and the intrusion lengths are also shown below each TEM micrograph. The inserts show a larger magnification of the silicide/Si interface.