Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 438-439

P-3-18

Electrical and Structural Evaluations of Ultrathin SiGe- and Ge-on-insulator Fabricated Using Ge Condensation by Dry Oxidation

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1. Introduction

Ge-on-insulator (GOI) structure is an attractive candidate for the fabrication of next-generation high-performance ultra large scale integration, because it has high carrier mobility and small parasitic capacitance. In particular, ultrathin GOI with the thickness of 10 nm or less is expected to improve device performance with further high drive current under ballistic transport as well as the advantage of ultrathin size effect [1]. An ultrathin GOI can be fabricated using Ge condensation by dry oxidation [2], which involves selective Si oxidation and Ge diffusion in SiGe layer.

In this work, we focused on crystal defect generation and channel hole mobility enhancement for ulthrathin SiGe-on-insulator (SGOI) and ultrathin GOI (~10 nm), which were fabricated using Ge condensation by dry oxidation. The crystal defects and channel hole mobility enhancement were observed by transmission electron microscopy (TEM) and Pseudo-MOSFET (Ψ-MOSFET) method [3], respectively.

2. Experiment, results and discussion

The specification of as-received wafer can be seen from Fig. 1(a), which was fabricated using Ge condensation by dry oxidation of intrinsic SiGe on 8-inch low-dosed separation-by-the-implanted-oxygen Si on insulator substrate by chemical vapor deposition method. An intrinsic strained Si layer was epitaxially grown on the 62 nm SiGe in the final step. The high quality of this as-received wafer was ensured by photoluminescence in our previous work [4].

We performed Ge condensation by dry oxidation in 100% O_2 atmosphere at temperatures as high as possible after considering melting point of SiGe, as shown in Fig. 1, which resulted in the formation of 27.5 nm $Si_{0.45}Ge_{0.55}$, 20.5 nm $Si_{0.25}Ge_{0.75}$ and 12.5 nm GOI, respectively. The thickness and Ge fraction of SGOI/GOI were measured by spectroscopic ellipsometry (SE) and TEM.

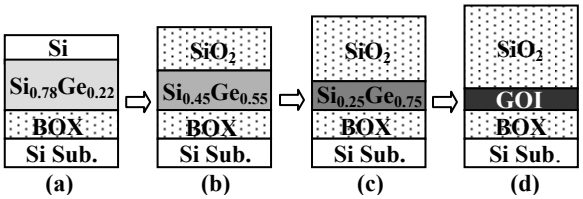

Fig. 1 GOI fabrication process by Ge condensation. (a) 62 nm $Si_{0.78}Ge_{0.22}$ as-grown sample; (b) 27.5 nm $Si_{0.45}Ge_{0.55}$ by oxidation from 1200 ^{0}C to 1075 ^{0}C for 28 min; (c) 20.5 nm $Si_{0.25}Ge_{0.75}$ by oxidation from 1075 ^{0}C to 950 ^{0}C for 30 min; (d) 12.5 nm GOI by oxidation from 950 ^{0}C to 900 ^{0}C for 5 min and 900 ^{0}C for 120 min.

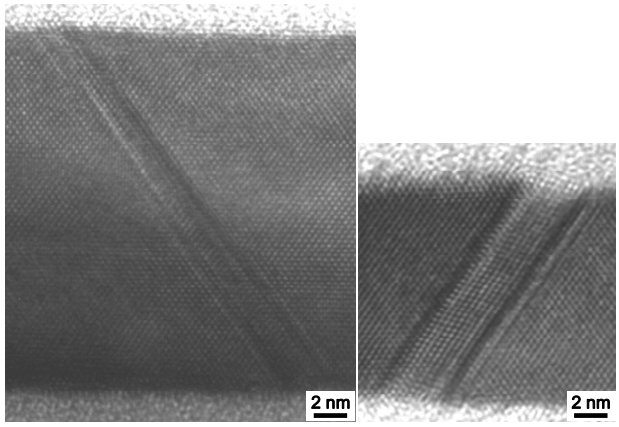

Fig. 2 Cross sectional TEM image. (a) $Si_{0.25}Ge_{0.75}$; (b) GOI.

The crystal quality of SGOI and GOI layers was evaluated by TEM, as shown in Fig. 2. The crystal structure of $Si_{0.45}Ge_{0.55}$ layer was perfect and no defect was observed in our visual field of several μms. With increasing Ge fraction, stacking faults generated in $Si_{0.25}Ge_{0.75}$ layer, as shown in Fig. 2(a), which extends from top SiO_2 to BOX layer. This kind of defect should be originated from strain relaxation and dislocation dissociation [5,6]. By applying the theory of stacking fault formation [6] to our sample, we calculated the critical Ge fraction for stacking fault formation, which is 63.5% for initial 62 nm $Si_{0.78}Ge_{0.22}$ layer. This result consists with experimental results of stacking fault formation in $Si_{0.25}Ge_{0.75}$ layer and defect absence in $Si_{0.45}Ge_{0.55}$ layer. In the 12.5 nm GOI layer, lattice image of Fig. 2(b) shows the defect is microtwin. Nakaharai et al. have reported the critical Ge fraction of 0.5 for the changes in defect structures from stacking fault to microwin [7], which is different from our present results. It is likely to be caused by the difference of initial thickness and Ge fraction of SGOI layer.

As to the electrical evaluation, we fabricated Ψ-MOSFET structure as shown in the inset of Fig. 3. Al film with the thickness of 100 nm was deposited on SGOI/GOI by evaporation and patterned by lift-off lithography as source and drain electrode. Then a mesa etching was performed for SGOI and GOI layers. Finally, Ohmic contact for source and drain was formed by annealing at 350 ^{0}C for 30 min in N_2 ambient.

In order to clarify the influence of top SiO_2 layer on channel properties, two kinds of Ψ-MOSFETs with and without top SiO_2 were fabricated. For all the samples, the accumulation-mode p-type Ψ-MOSFET operation with good linear and saturation regions was confirmed by the drain current I_D versus drain voltage V_D measurement.

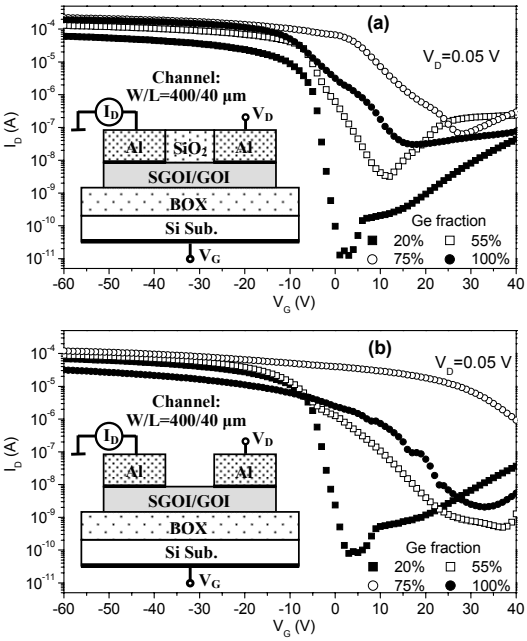

Fig. 3 I_D-V_G characteristics with various Ge fraction. (a) with top SiO_2; (b) without top SiO_2. The inset shows Ψ-MOSFET structure.

Fig. 3 shows I_D versus gate voltage V_G characteristics with various Ge fractions. The off-leakage current of $Si_{0.8}Ge_{0.2}$ is very low due to its small hole concentration. For $Si_{0.25}Ge_{0.75}$, off-leakage current, bulk current, and channel inversion voltage are relative high as compared to $Si_{0.45}Ge_{0.55}$ and GOI, which should be attributed to the fact that the number of hole induced by the defect-generation is much higher than those of $Si_{0.45}Ge_{0.55}$ and GOI.

The channel hole mobility can be extracted from I_D-V_G characteristics in the linear I_D-V_D region by using following formula [3]:

$$\frac{I_D}{\sqrt{g_m}} = \sqrt{f_g C_{ox} V_D \mu_0}(V_G - V_{FB})$$

where g_m is transconductance, f_g the geometric coefficient, C_{ox} the BOX layer capacitance, V_{FB} the flat-band voltage for accumulation channel, and μ_0 the low field hole mobility. For this method of μ_0 extraction, I_D should be a pure channel current. Thus, the bulk current should be subtracted from the measured I_D. The extracted μ_0 and flat-band voltage are shown in Fig. 4 and listed in Table I, respectively. It is very clear that μ_0 is effectively enhanced with increasing Ge fraction for the sample with top SiO_2.

The values of μ_0 for $Si_{0.8}Ge_{0.2}$ and $Si_{0.45}Ge_{0.55}$ without top SiO_2 are almost the same as those with top SiO_2. On the contrary, the values of μ_0 for $Si_{0.25}Ge_{0.75}$ and GOI without top SiO_2 drastically decreased relative to those with the top SiO_2, especially for GOI sample. This means that the top surface for the very thin SGOI and GOI significantly affects to the back-side channel mobility, suggesting that the remote Coulomb scattering is caused by the high surface states density. Therefore, the top surface passivation is very important for the μ_0 evaluation for ultrathin SGOI and GOI samples.

As to the samples with comparably thick SGOI layer, the high surface state density is likely to be negligible. In fact, high hole mobility for thick GOI layer (30 nm) without top SiO_2 [8] was reported by Maeda et al.

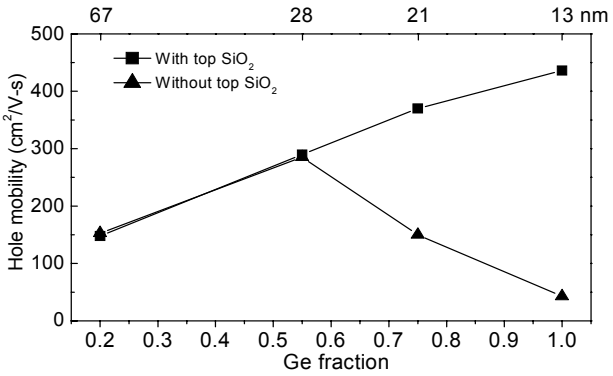

Fig. 4 Hole mobility dependence on Ge fraction. 67 nm $Si_{0.8}Ge_{0.2}$ sample was obtained after a dry oxidation at 1000 ^{0}C for 10 min, which is the same as in Ref. [4].

V_{FB} also strongly depends on the interface properties of top-SiO_2/SGOI and SGOI/BOX, which were summarized in Table 1. There is a positive-shift tendency of V_{FB} with increasing Ge fraction, except the one of GOI with top SiO_2. This shift should be attributed to the existence of negative interface charges with high density [9]. However, further studies are necessary to clarify its origin.

Table I Flat-band voltage.

Ge fraction	0.2	0.55	0.75	1.0
V_{FB} (V) (With top SiO_2)	-5.2	-5.6	-0.8	-15.0
V_{FB} (V) (Without top SiO_2)	-4.8	-6.0	-0.2	1.6

3. Conclusion

Defect generation of stacking fault and microtwin during Ge condensation process was observed by TEM. The μ_0 was investigated for SGOI with various Ge fractions and thicknesses by Ψ-MOSFET method. The μ_0 enhancement for SGOI/GOI with top SiO_2 was clear with increasing Ge fraction. However, ultrathin SGOI without top SiO_2 showed degradation of μ_0, which suggests that the influence of top surface states become very strong with decreasing thickness of SGOI layer.

Acknowledgements

This study was partially supported by STARC.

References

[1] S. Takagi, *VLSI Tech. Dig.* (2003) 115.
[2] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama and S. Takagi, Appl. Phys. Lett. **83** (2003) 3516.
[3] S. Cristoloveanu, D. Munteanu and MS. T. Liu, IEEE Trans. Electron Dev. **47** (2000) 1018.
[4] D. Wang, K. Matsumoto, M. Nakanae and H. Nakashima, Appl. Phys. Lett. **87** (2005) 251928.
[5] S. W. Bedell, K. Fogel, D. K. Sadana and H. Chen, Appl. Phys. Lett. **85** (2004) 5869.
[6] B. Vinent., J. -F. Damlencourt, V. Delaye, R. Gassilloud, L. Clavelier and Y. Morand, Appl. Phys. Lett. **90** (2007) 074101.
[7] S. Nakaharai, T. Tezuka, N. Hirashita, E. Toyoda, Y. Moriyama, N. Sugiyama and S. Takagi, Semicond. Sci. Technol. **22** (2007) S103.
[8] T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama and S. Takagi, IEEE Electron Device Lett. **26** (2005) 102.
[9] T. Tezuka, N. Sugiyama, T. Mizuno and S. Takagi, IEEE Trans. Electron Dev. **50** (2003) 1328.