P-3-19

# Triple-gate FinFETs with Fin-thickness Optimization to Reduce the Impact of Fin Line Edge Roughness

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**Introduction:** Intra-die fluctuations in the nanoscale CMOS technology emerge due to intrinsic parameter fluctuations induced by line edge roughness (LER) [1]. LER can cause the random deviation of the line edge from its ideal pattern and it does not reduce with scaling down of line width [2]. FinFET is a promising candidate that can be applied into sub-30nm technology with good ability to suppress the short channel effects (SCEs) [3]. However, to reduce fluctuations of FinFETs performance is still imperative [4] and the strongest fluctuations are introduced by the fin LER [5]. As the fin is conventionally designed less than one third of the channel length to suppress SCEs [6], it imposes a big challenge on the lithography and etching. Here we propose to relax the fin-thickness constraints in order to reduce the influence of intra-die fluctuations. Through our 3-D simulation, we suggest using triple-gate FinFETs with optimized fin-thickness to minimize the fin LER effects, meanwhile to suppress SCEs under a tolerable degree.

**Device Structure and Simulation Method:** Fig. 1 shows the device structure of triple-gate FinFETs with fin LER. The geometrical and doping parameters used in simulation are listed in Table 1. Fin roughness is generated by a Fourier analysis of the Gaussian autocorrelation function introduced in our earlier work [7]. Fig. 2 is schematic of the flow to generate the random sequence. The properties of FinFETs we consider include threshold voltage Vt,lin at Vds=50mV and Vt,sat at Vds=1V; the value of the drain induced barrier lower effect (DIBL) defined as (Vt,lin-Vt,sat)/ $\Delta$Vds; drive current $I_{on}$ and leakage current $I_{off}$. Hundreds of 20nm double-gate (DG) and triple-gate (TG) FinFETs with different fin-thickness (Tsi) are simulated in 3-D by ISE-TCAD tools [8]. Since LER does not reduce with scaling down of line width [2], we assume all the samples have the same rms amplitude (1nm) of fin LER in spite of different Tsi. Fisrtly, FinFETs with smooth line edge (referred as ideal) are evaluated. Then FinFETs with fin LER (referred as rough) are simulated to investigate their properties' shifts (evaluated by average value Avg) and fluctuations (evaluated by standard deviation $\sigma$). In order to achieve statistical stability, all the simulations have an ensemble size of 100. Quantum effect is taken into account by density-gradient method.

**Results and Discussion:** Fig. 3 shows that with the increase of Tsi, ideal FinFETs' Vt,lin decreases almost linearly while Vt,sat drops dramatically. The outcome of SCEs is unavoidable because the gate controllability of the front and back gates reduces when fin is widened. However, TG structure performs better than DG structure in the suppression of the SCEs due to the top gate's control over channel. Fig. 4 plots ideal FinFETs' DIBL value as a function of Tsi, showing TG devices' advantage to suppress SCEs when fin is widened. Fig. 5 shows that with the increase of Tsi, ideal FinFETs' $I_{on}$ rises almost linearly and $I_{off}$ rises almost exponentially. It is noticed that TG devices' benefits such as larger drive current and smaller leakage current do not appear until Tsi exceeds half the channel length (10nm). Fig. 6 shows that fin LER contributes to a remarkable increase of threshold voltage, and the thinner the fin is, the more Vt,lin shifts. This is because the quasi-continuous conduction band splits into a series of discrete sub-bands due to quantum confinement effect. The thinner the fin is, the more notable this effect becomes. Fig. 6 also shows with the same Tsi, Vt,lin's shifts are less remarkable in TG devices than in DG devices. Thus, TG FinFETs with wider fin present a potential ability to reduce fin LER effects. However, widening the fin should be treated carefully, for it may exacerbate the SCEs as shown in Fig. 7. Fortunately, DIBL does not rise as aggressively as expected in TG devices, noting that in Fig. 7 rough FinFETs with TG structure have a lower DIBL than that of ideal FinFETs. Another drawback of widening fin is the exponentially increase of leakage current as shown in Fig. 8. However, the leakage current of rough FinFETs does not rise as aggressively as expected in ideal FinFETs because fin LER contributes to a significant increase of threshold voltage. Additionally, it can be seen in Fig. 8 that when fin is thin, TG devices even have a larger $I_{off}$ than DG devices, because at this region $I_{off}$ is dominated by gate leakage current rather than sub-threshold leakage current, and TG devices have a relatively larger area of gate. TG devices' superiority in lowering leakage current does not appear until the fin is wide enough (eg. 20nm). Fig. 9 shows that with the increase of Tsi, the fluctuations of Vt,lin drop almost linearly. Also TG devices present better consistency of threshold voltage under the influence of fin LER. Fig. 10 shows that with the increase of Tsi, the fluctuations of DIBL drop dramatically. Although the absolute value of DIBL increases when the fin is widened, the variation is weakened. The similar phenomenon can be observed in Fig. 11, which shows that with the increase of Tsi, the fluctuations of leakage current drop dramatically. Moreover, in Fig. 10 and Fig. 11, TG devices present superiority to DG devices in the suppression of the SCEs such as the increase of DIBL and leakage current. In summary, widening the fin inevitably brings about SCEs. However, using TG devices instead of DG devices can achieve better resistance to SCEs because of the top gate's control over the channel. What makes more sense is that widening the fin can significantly reduce the shifts and fluctuations of device performance caused by fin LER effects. From our simulation above, we suggest relaxing fin-thickness constraints from less than one third of the channel length to half or even equal to the channel length. With the help of TG structure, FinFETs with optimized fin-thickness can reduce the influence of fin LER meanwhile suppress SCEs under a tolerable degree.

**Conclusion:** By 3-D statistical simulation, we investigate the effects brought by widening the fin of ideal FinFETs with smooth line edge and rough FinFETs with fin LER. The results show that the benefits of widening fin to reduce shifts and fluctuations caused by fin LER outweigh the detriment of possibly enhanced SCEs. So we propose to relax the fin-thickness constraints to achieve better resistance to fin LER effects. In the meantime, we propose to use triple-gate FinFETs to replace the conventional double-gate FinFETs to help suppress SCEs after fin is widened. Our simulation provides guidelines for designing FinFETs device to reduce intra-die fluctuations.

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**Reference:**

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[7] S. Yu, et al, in *Silicon Nanoelectronics Workshop*, 2008.
[8] ISE-TCAD tools from Integrated System Engineering (ISE).

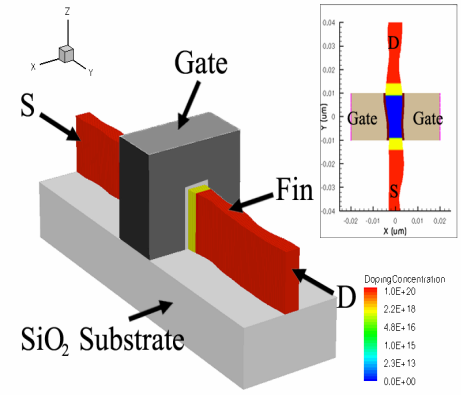


Fig. 1 3-D schematic of triple-gate FinFET with fin LER. The inset is the 2-D cross section sliced at half fin-height, showing the fin LER.

| *PARAMETER* | *VALUE* |
|---|---|
| channel length | 20 nm |
| fin-height | 20 nm |
| fin-thickness | 5, 10, 20nm |
| EOT | 1 nm |
| channel doping | intrinsic |
| S/D doping | n-type $10^{20}$ $cm^{-3}$ |
| S/D extension doping | n-type $10^{18}$ $cm^{-3}$ |
| gate metal work function | 4.5 eV |

Table 1 Simulated FinFETs' geometrical and doping parameters.

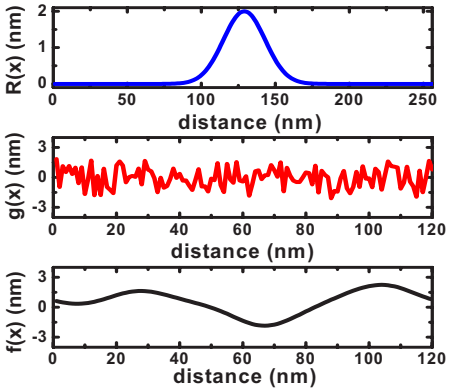


Fig. 2 Example of random sequence generation flow. Inputs are Gaussian autocorrelation function R(x) and white noise g(x). Output f(x) is used to simulate LER.

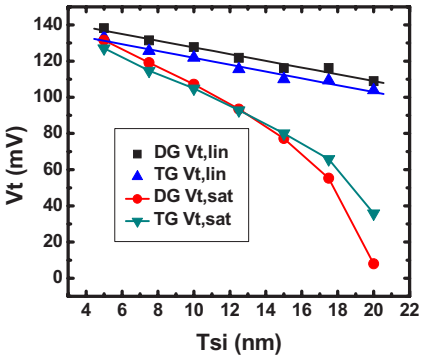


Fig. 3 Ideal threshold voltage (Vt,lin and Vt,sat) of DG and TG FinFETs as a function of fin-thickness (Tsi).

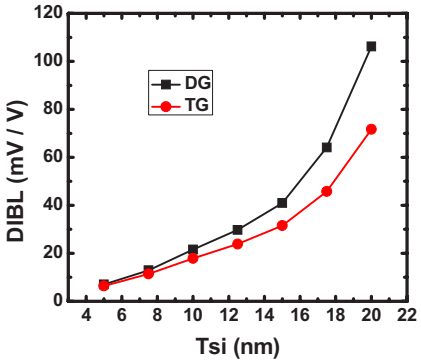


Fig. 4 Ideal DIBL value of DG and TG FinFETs as a function of fin-thickness (Tsi).

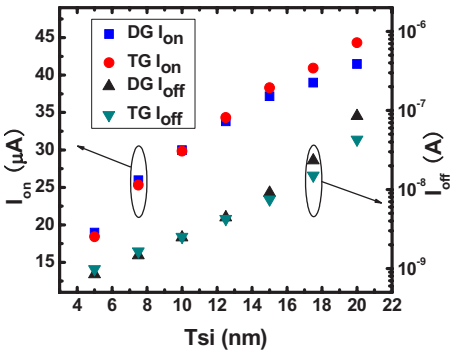


Fig. 5 Ideal drive current ($I_{on}$) and leakage current ($I_{off}$) of DG and TG FinFETs as a function of fin-thickness (Tsi).

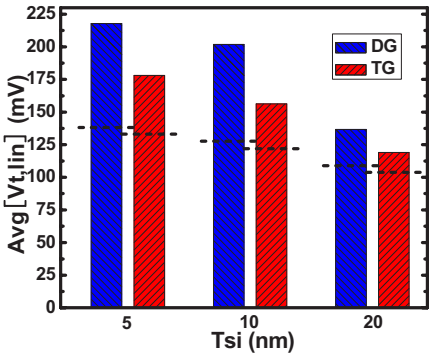


Fig. 6 Shifts of threshold voltage (Vt,lin) of DG and TG FinFETs as a function of fin-thickness (Tsi). The dashed lines are Vt,lin of ideal FinFETs.

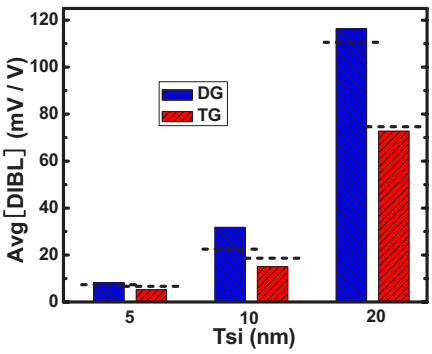


Fig. 7 Shifts of DIBL value of DG and TG FinFETs as a function of fin-thickness (Tsi). The dashed lines are DIBL of ideal FinFETs.

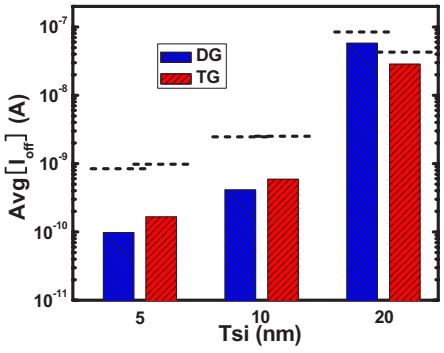


Fig. 8 Shifts of leakage current ($I_{off}$) of DG and TG FinFETs as a function of fin-thickness (Tsi). The dashed lines are $I_{off}$ of ideal FinFETs.

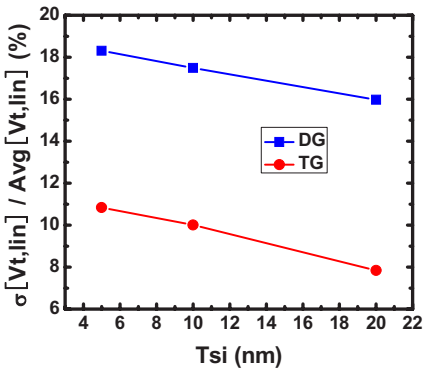


Fig. 9 Fluctuations of threshold voltage (Vt,lin) of DG and TG FinFETs as a function of fin-thickness (Tsi).

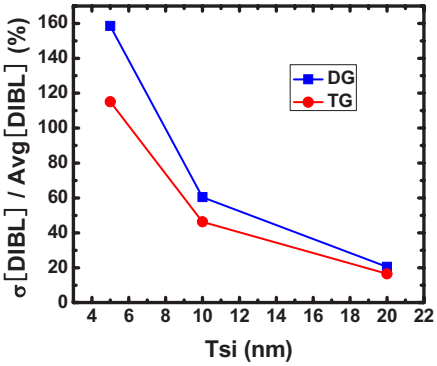


Fig. 10 Fluctuations of DIBL value of DG and TG FinFETs as a function of fin-thickness (Tsi).

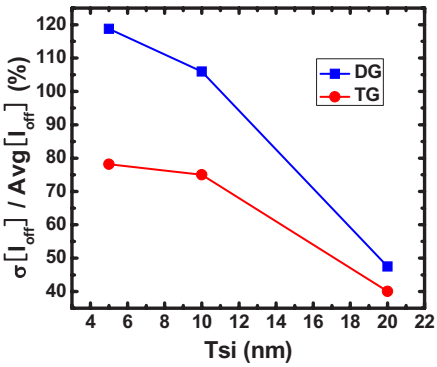


Fig. 11 Fluctuations of leakage current ($I_{off}$) of DG and TG FinFETs as a function of fin-thickness (Tsi).