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Analysis of Fowler-Nordheim Stress Induced Trap Generation on Random Telegraph Signal Noise

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***Abstract*—From the viewpoint of random telegraph signal noise, general form of random telegraph signal noise is changed to complex form because of electrical stress in gate dielectric. Especially, in case of flash memory, Fowler-Nordheim tunneling is used in common operation. In this paper, various Fowler-Nordheim tunneling stresses induced oxide traps generation is investigated by using random telegraph signal noise analysis.**

1. Introduction

As CMOS devices are down-scaled, the effect of an individual defect on device performances becomes more serious. In sub-micron MOSFET, the random telegraph signal (RTS) noise, which is characterized by discrete switching events of the channel current, is observed through the trapping and de-trapping of conduction carriers in individual interfacial defects [1], [2]. If the trap energy level is within a few kT of the electron Fermi-level, trapping phenomenon takes place [3].

The RTS noise is important for scientific study as it has been considered to be the origin of flicker noise and provides valuable information pertinent to carrier transport behavior [4]. The characteristics of semiconductor devices are degraded due to the generation of oxide traps by the electrical stress. In this paper, Fowler-Nordheim (FN) tunneling stress induced oxide trap generation is investigated using the RTS noise analysis.

2. Noise Analysis

The conventional RTS noise model is based on only the ratio of electron capture and emission time. In this work, the two effects included model is used, that is the poly gate depletion effect and surface potential variation in strong inversion regime [4]. The RTS noise model with consideration of the two effects is given as follows.

$$x_T = \frac{T_{ox}\left(\frac{d\psi_S}{dV_{gs}} + \frac{KT}{q}\frac{d\ln(\tau_c/\tau_e)}{dV_{gs}}\right)}{\frac{d\psi_P}{dV_{gs}} + \frac{d\psi_S}{dV_{gs}} - 1} \quad (1)$$

where τ_c and τ_e are average capture and emission time, respectively. And, ψ_S and ψ_P are the amount of band banding in channel and gate poly-gate dielectric surface. Also, x_T represents for the position of trap in the oxide. T_{ox} is the oxide thickness and V_{gs} is the gate voltage.

3. Results and Discussion

The nMOSFETs with the gate width/length of W/L = 2/0.13 μm have been used in this work. Electrical T_{ox} is about 3 nm. FN stresses of 10, 11 and 12 MV/cm are applied to generate oxide traps intentionally.

Figs. 1(a), (b) and (c) show the RTS noise time domain data as stress time. To generate the traps, electric field of 10 MV/cm was applied on the gate oxide for 10,000 sec. In this manner, 8000 sec and 500 sec were needed from 11 and 12 MV/cm FN stress, respectively. From the RTS noise time domain data with various gate voltage, $d\ln(\tau_c/\tau_e)/dV_{gs}$ could be extracted through liner fitting as shown in Fig. 2. The x_T of process induced traps and FN stress induced traps was calculated by using Eq. (1) and $d\ln(\tau_c/\tau_e)/dV_{gs}$ data in each sample. As shown in Fig. 3, $d\psi_P/dV_{gs}$ and $d\psi_S/dV_{gs}$ are extracted as 0.01892 and 0.07214 for Eq. (1). The calculated results are summarized in Table I. The stress induced traps are located closer to Si-SiO_2 surface than process induced traps. Actually, τ_c and τ_e of stress induced traps are faster and this is true according to theorem of fast and slow traps [5].

The distance between process and stress induced trap depth was calculated for different FN stress conditions as shown in Fig. 4. It is observed that the stress induced trap is generated closer to the process induced trap as increasing the electric field.

Therefore, the initial process induced traps can play an important role in the MOS device such as NAND flash memories, in which the FN stress is used for both program and erase operation.

4. Conclusions

The oxide trap depth has been investigated with RTS noise. It is found that the stress induced traps are closely positioned to the Si-SiO_2 interference than the process induced traps. It is further observed that the newly generated traps by the FN stress are located near the process induced traps. Therefore, reducing the process induced traps is important in the MOS device such as NAND flash memory devices.

Acknowledgement

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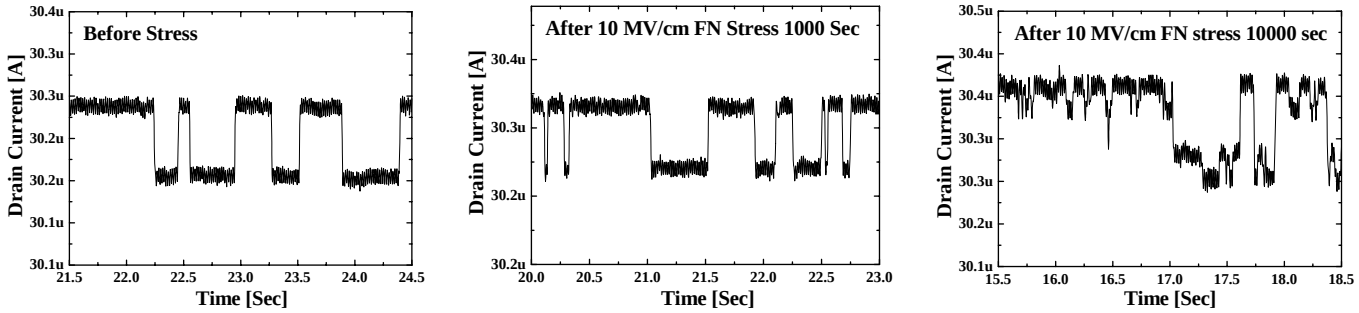
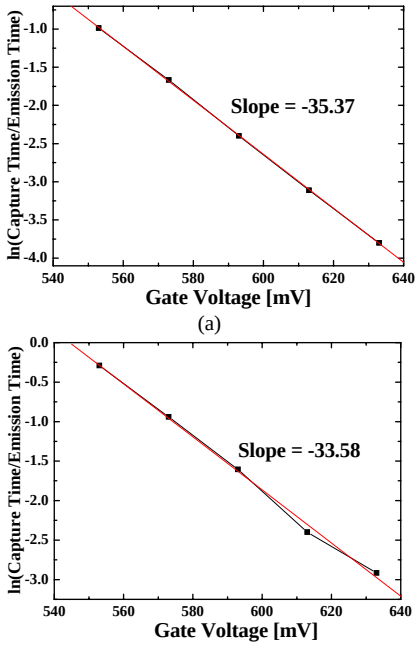


(a) (b) (c)

Fig. 1. The time domain RTS noise of drain current. Before stress state, the general two level RTS noise was observed. (a) After 1,000 sec stress with the electric field of 10 MV/cm, the two level RTS noise was still observed. (b) However, complex RTS noise was observed after 10,000 sec stress with the electric field of 10 MV/cm.



(a)

(b)

Fig. 2. The gate voltage vs. $\ln(\tau_c/\tau_e)$. For (a) the process and (b) stress induced (11 MV/cm) traps.

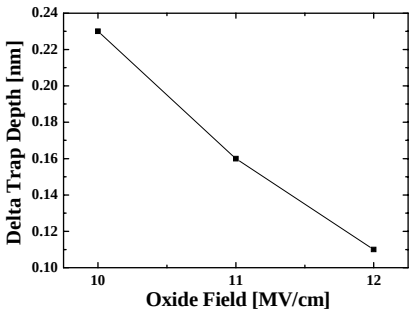
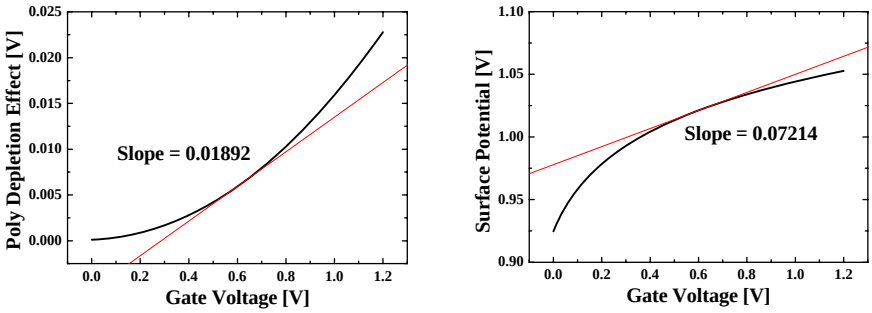


Fig. 4. The distance between process and stress induced trap depth the electric field.



(a) (b)

Fig. 3. (a) Calculated poly depletion effect and (b) surface potential as a function of gate voltage.

Table I. Calculated trap depth.

	10 MV/cm	11 MV/cm	12 MV/cm
Process induced trap depth	1.96 nm	2.77 nm	2.69 nm
Stress induced trap depth	1.73 nm	2.61 nm	2.58 nm