1. Introduction

Recently, much effort has been made to integrate high-voltage devices into advanced CMOS and BiCMOS technologies [1]-[4]. Lateral DMOS (LDMOS) transistors are the suitable devices to be integrated because of their compatibility with CMOS technology. Thus, the characterization, optimization, and hot-carrier reliability of LDMOS devices have been widely studied [5]-[8]. In this work, hot-carrier reliability in n-type LDMOS transistors with shallow trench isolation (STI) in drift region is investigated. Although on-resistance (\(R_{on} = V_{ds}/I_d\)) increases as the stress time increases, an unexpected reduction in \(R_{on}\) is observed at the beginning of stress. Based on experimental data and TCAD simulation results, the mechanisms responsible for \(R_{on}\) shift are discussed.

2. Experiments

The schematic cross section of the n-type LDMOS transistor used in this work is shown in Fig. 1. This device is integrated into a 0.25\(\mu\)m CMOS process and features a STI in n-type drift region near the drain. The channel length is about 0.3\(\mu\)m and the width is 10\(\mu\)m. The operational voltages are \(V_{ds} = 40\) V and \(V_{gs} = 12\) V. To investigate hot-carrier reliability of the device, DC stressing under \(V_{ds} = 40\) V and various \(V_{gs}\) is performed at room temperature with source and bulk connected to the ground. The stress tests are interrupted periodically to measure the degradation of device parameters. Two-dimensional TCAD simulation is also performed to explain the experimental results.

3. Results and Discussion

Two substrate current (\(I_{sub}\)) peaks are observed in \(I_{sub}-V_{gs}\) characteristics in our LDMOS devices. The first \(I_{sub}\) peak occurs at \(V_{gs} = 4\) V that is similar to the behavior in conventional MOSFETs. As \(V_{gs} > 8\) V, \(I_{sub}\) rises again because of Kirk effect [8] and the second \(I_{sub}\) peak occurs at \(V_{gs} = 12\) V. When the devices are stressed under \(V_{ds} = 40\) V with various \(V_{gs}(2.5, 4, 8, \text{and } 12\) V), the device stressed under \(V_{gs} = 12\) V degrades the most. As a result, the following analysis is focused on the device stressed under \(V_{gs} = 12\) V. Fig. 2 shows linear-region \(I_d\) (measured at \(V_{ds} = 0.1\) V) vs. \(V_{gs}\) before and after stress for the device stressed under \(V_{ds} = 40\) V and \(V_{gs} = 12\) V for 3000 s. A slight increase in \(I_d\) is found when the device is stressed for 1 s, while \(I_d\) decreases when the device is stressed for 3000 s. Such a phenomenon can also be seen in Fig. 3, where the shift in \(R_{on}\) (measured under \(V_{ds} = 0.1\) V and \(V_{gs} = 12\) V) vs. stress time for the device in Fig. 2 is drawn. When the stress time is less than 10 s, \(R_{on}\) is smaller than its fresh value (\(I_d\) increases). As the stress time is longer than 10 s, \(R_{on}\) is greater than its fresh value (\(I_d\) decreases).

To investigate the mechanism of \(R_{on}\) degradation, results of TCAD simulation are analyzed. Fig. 4 shows simulated impact ionization (ii) rate along Si/SiO\(_2\) interface when the device is biased at \(V_{ds} = 40\) V and \(V_{gs} = 12\) V. It is clear that an ii peak exists at the bottom-left corner of STI. Another severe ii generation caused by Kirk effect occurs at the right-side of STI. Fig. 5 shows simulated vertical electric field (\(E_y\)) along the same cut-line as in Fig. 4 under the same bias condition. Positive \(E_y\) is favorable for hole injection. Negative \(E_y\) is favorable for hole injection. From Figs. 4 and 5, the mechanisms of \(R_{on}\) degradation are suggested as follows. At the bottom-left corner of STI, energetic electron-hole pairs are generated because of ii generation. Holes are injected into STI because of negative \(E_y\). Such a hot-hole injection may create hole trapping and interface trap (\(N_{it}\)). Trapping of holes in STI induces negative mirror charges at Si/SiO\(_2\) interface in drift region, resulting in an effective increase in drift region concentration. As a result, \(I_d\) increases and \(R_{on}\) decreases [9]. This inference explains why \(R_{on}\) is smaller than its fresh value at the beginning of stress. On the other hand, the severe ii generation at the right-side of STI results in hot-electron injection because of positive \(E_y\). Such an electron injection may create electron trapping and \(N_{it}\), leading to \(R_{on}\) increase. The damage created at the right-side of STI is expected to dominate \(R_{on}\) degradation as the stress time is longer. This explains why \(R_{on}\) is greater than its fresh value after 10 s as in Fig. 3.

To verify the existence of hole trapping, Fig. 6 shows \(I_d\) shift measured at different \(V_{gs}\) vs. stress time for the device in Fig. 2. When \(I_d\) is measured at low \(V_{gs}(V_{gs} = 3.5\) V), the current path under STI is deeper. This argument can be confirmed in Fig. 5, where the simulated accumulated current as a function of the depth from Si/SiO\(_2\) interface at the location of bottom-left corner of STI is shown. The current is accumulated from the bottom of N region to Si/SiO\(_2\) interface. It is clear that the accumulated current near Si/SiO\(_2\) interface under \(V_{gs} = 3.5\) V rises less rapidly than that under \(V_{ds} = 12\) V, indicating that current path is away from Si/SiO\(_2\) interface at low \(V_{gs}\). As current flows deeper, the effect of negative mirror charges on \(I_d\) decrease is less apparent. Thus, \(I_d\) decreases monotonously during stress when \(I_d\) is measure at \(V_{gs} = 3.5\) V as in Fig. 6. The results in Fig. 6 reveal that hole trapping is responsible for the unexpected \(R_{on}\) reduction in the early stage of stress.

4. Conclusions

N-type LDMOS transistors stressed under the \(V_{gs}\) to produce the worst device degradation is discussed. \(R_{on}\) decreases at the beginning of stress but \(R_{on}\) increases afterwards. \(R_{on}\) reduction is attributed to hole-injection and trapping at the bottom-left corner of STI. As the stress time increases, damage created by hot-electron injection at the right-side of STI leads to \(R_{on}\) increase.

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References

Fig. 1 Schematic cross section of the n-type LDMOS device.

Fig. 2 Linear-region $I_d$ vs. $V_{gs}$ before and after stress for the device stressed under $V_{ds} = 40$ V and $V_{gs} = 12$ V for 3000 s.

Fig. 3 $R_{on}$ shift vs. stress time for the device stressed under $V_{ds} = 40$ V and $V_{gs} = 12$ V.

Fig. 4 Impact ionization rate along Si/SiO$_2$ interface under $V_{ds} = 40$ V and $V_{gs} = 12$ V.

Fig. 5 Vertical electric field along Si/SiO$_2$ interface under $V_{ds} = 40$ V and $V_{gs} = 12$ V.

Fig. 6 $I_d$ shift measured at different $V_{gs}$ vs. stress time.

Fig. 7 Accumulated current vs. the depth from Si/SiO$_2$ interface at the location of bottom-left corner of STI.