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Impact of Tungsten Capping Layer on Yttrium Silicide for Low Resistance Source/Drain Contacts

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I. Introduction

Source/drain parasitic resistance R_{SD} of MISFETs is a serious problem because it will limit their performance when the current drivability increases sufficiently. In order to reduce R_{SD}, it is important to reduce contact resistance. As the Schottky Barrier Height (SBH) between silicide and silicon must be low to achieve low contact resistivity [1], a dual silicide structure, using low work function silicides for n^+ silicon and high work function silicides for p^+ silicon, is a promising solution [2]. However, it is difficult to obtain low SBH for electrons because it requires handling low work function metals, which are easily oxidized in air. Therefore, the oxidation prevention technology is indispensable. In this paper, we investigated the physical and electrical properties of tungsten/yttrium stack.

II. Experimental

In order to fabricate a Schottky barrier diode (SBD), n on n^+ and p on p^+ epitaxially grown Si(100) wafers were prepared. A-300nm-thick field oxide layer was formed at 1,100°C by wet oxidation. Typically 1mm×1mm square shaped windows were opened in the field oxide. Then the wafers were cleaned by using total room temperature 5 step cleaning [3]. Then the wafers were loaded into an N_2 sealed cleaning and transfer system, whose detail has already reported [4]. After the samples were loaded into a clustered sputter chamber, A 10-nm-thick yttrium film and a 300-nm-thick tungsten film were sequentially formed by rf sputtering deposition, followed by lamp annealing to form yttrium silicide. Sputtering conditions are listed in Table 1. After the electrode patterning was formed by chemical etching technique, back contact was formed by thermally Al evaporation. The schematic view of the fabricated SBD is shown in Fig. 1. The SBH was evaluated mainly from current voltage and current temperature characteristics.

III. Results and Discussions

Fig. 2 shows the scanning electron microscopy (SEM) image of tungsten/yttrium stack after annealing at 500°C for 2min in Ar ambient. The two layers are easily distinguished even after heat treatment. Fig. 3 shows x-ray photoelectron spectroscopy (XPS) depth profiles of tungsten, yttrium, silicon, and oxygen. From these spectra, it is clear that yttrium and silicon are not detected in upper tungsten capping layer. Oxygen is detected only at the surface of tungsten layer and not found in the yttrium silicide layer. These results show that tungsten layer can effectively work as a capping layer, which can prevent yttrium from being oxidized. However, we must point out that based on secondary ion mass spectroscopy (SIMS) depth profile shown in Fig. 4, a little amount of tungsten is detected in yttrium silicide layer, maybe due to diffusion along the grain boundary. Fig. 5 shows the x-ray diffraction (XRD) patterns of tungsten/yttrium stack as a function of the annealing temperature. The peak from yttrium disilicide is detected over 300°C up to 700°C. This result is consistent with other literature [5]. No other notable peaks are detected between these temperatures. Fig. 6 shows the current voltage characteristics of tungsten /yttrium silicide stacked SBD for p-type silicon as a function of measurement temperature. A very low reverse-biased current, as low as 3×10^{-7}A/cm^2 is obtained at 298K. An n-value extracted from forward characteristics is around 1.02, which implies good interface properties between yttrium silicide and silicon. For n-type silicon, the characterisitics are completely ohmic at room temperature because of its low SBH for electrons. Fig. 7 shows the current-temperature characteristics of the same samples as shown in fig. 6. Calculated curves based on simple thermionic emission (TE) theory [1] are also shown. The experimental data for both n- and p-type silicons are well fitted by TE theory, and extracted SBH are 0.311 eV for electrons and 0.756 eV for holes, respectively. The extracted SBH as a function of silicide formation temperature is shown in Fig. 8. Low SBH for electrons as around 0.31eV is obtained from 450°C to 650°C. Finally, It should be noted that tungsten capping layer employed in this paper can be applied to another rare-earth materials. Fig. 9 shows the current-voltage characteristics and the cross-sectional SEM image of tungsten/erbium stack after annealed. From current voltage characteristics, A good rectifying property is observed, as yttrium silicide.

IV. Conclusion

We have investigated the physical and electrical properties of tungsten/yttrium stack. Tungsten layer on low work function metals effectively works as a oxygen blocking cap. Fabricated SBD showed a near ideal JV characteristics, and extracted SBH is 0.31eV and 0.76eV for electrons and holes, respectively. We also confirmed that tungsten capping layer can be applied to other rare-earth metals, such as erbium. This result can be applied to the formation of source/drain contacts having

low contact resistivity and will improve the performance of MISFETs.

Acknowledgments

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Table 1 Sputtering conditions of yttrium films. The condition of tungsten deposition is almost the same, except for a DC bias applied to the target to enhance the deposition rate.

Gas	Ar
Flow Rate	432 sccm
Working Pressure	1.3 Pa (10mTorr)
Base Pressure	< 3x10^{-7} Pa
Substrate Temperature	RT
RF Power	100W
Frequency	100MHz

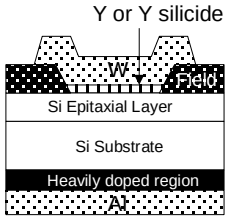

Fig. 1 Schematic view of tungsten /yttrium stacked Schottky barrier diode. The resistivity of the epitaxial silicon layer is about 10 Ωcm for both p- and n- type silicon.

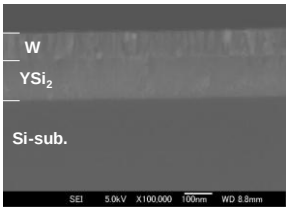

Fig. 2 Cross-sectional SEM image of W/ YSi_x stack after annealed at 500°C for 2min.

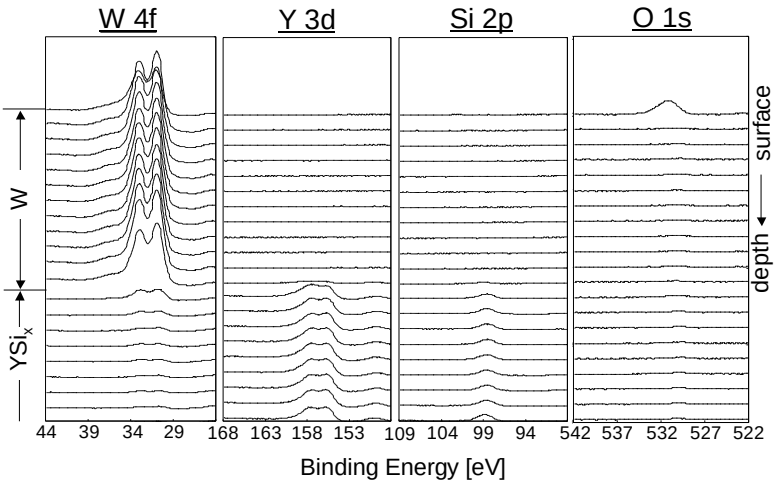

Fig. 3 XPS depth profiles of tungsten/yttrium stack after annealed at 500°C for 2min in Ar ambient. Yttrium and silicon are not found in upper tungsten layer, while they are simultaneously detected under tungsten layer, which indicates that silicidation of yttrium occurred without reacting with upper tungsten layer. Note that oxygen is detected only on the top of tungsten layer.

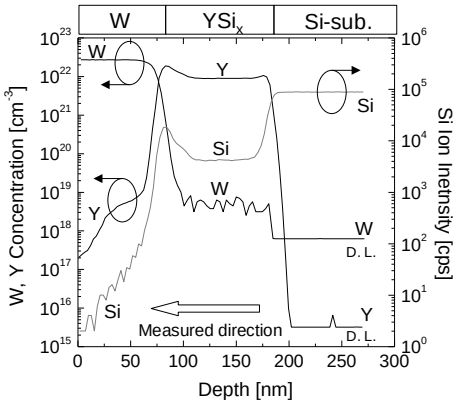

Fig. 4 SIMS depth profile of tungsten/yttrium stack after annealed at 500°C, 2min. This measurement was performed from substrate side toward the surface in order to avoid the knocking on effect. The concentration is valid only in silicon layer, because of the matrix effect. D. L. in the figure represents Detection Limit.

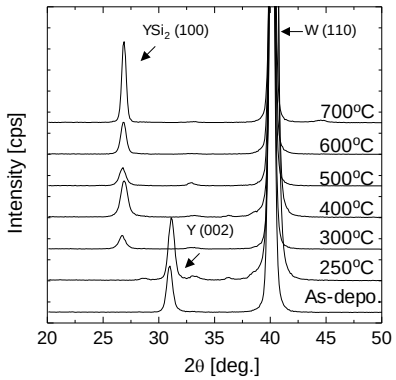

Fig. 5 XRD spectra of W(50nm) / Y(30nm) stack as a function of annealing temperature. Annealing time is 10min. Yttrium reacts with silicon over 300°C and is stable up to 700°C

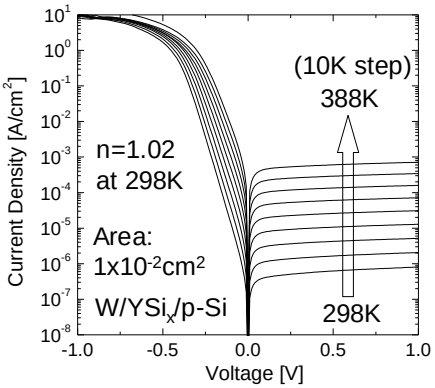

Fig. 6 Current Density-Voltage characteristics of W(300nm) /Y(10nm) stack Schottky barrier diode after annealed at 500°C as a function of measurement temperature.

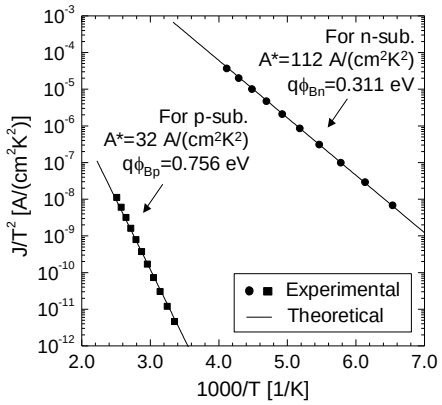

Fig. 7 J/T^2-1/T characteristics of fabricated W/YSi_x SBD for both p- and n-type substrate formed at 500°C. Theoretical curves based on TE theory are also shown.

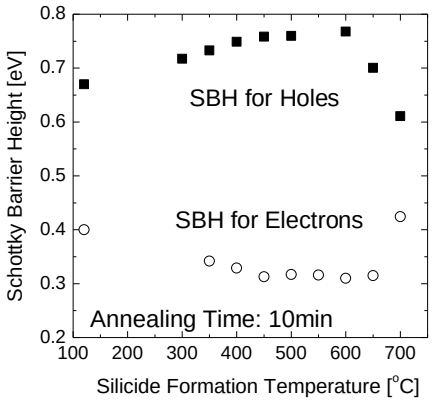

Fig. 8 Extracted SBH for both electrons and holes from reverse bias current at 0.1V of fabricated SBD. The sum of them is close to the bandgap of silicon. under ~600°C.

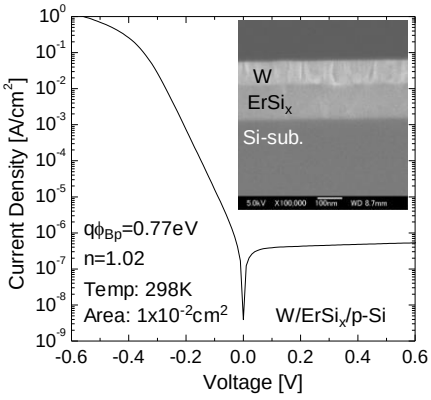

Fig. 9 Current-Voltage characteristics of tungsten /erbium silicide stacked Schottky barrier diode for p-type substrate. Silicide was formed at 500°C for 10min. Inserted figure was the SEM image of W/ErSix stack