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Multiple-gated Poly-Si Nanowire Thin-Film Transistors

Ta-Wei Liu[1], Hsing-Hui Hsu[1], Zer-Ming Lin[1], Chuan-Ding Lin[2], Tiao-Yuan Huang[1], Horng-Chih Lin[1, 2]

[1]Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University
[2]National Nano Device Laboratories, 1001 Ta Hsueh Road, Hsinchu, Taiwan 300, ROC

1. Introduction

Poly-Si thin-film transistors (TFTs) exhibit much higher carrier mobility and current drive over the amorphous Si counterparts, thus are attractive for a number of applications. However, it is also well known that the device performance is seriously affected by the granular structure of the poly-Si layer[1]. In this regard, the adoption of nanowire (NW) structures is feasible to reduce the impact by dramatically reducing the amount of defect contained in the channel. Recently, we have proposed a simple method to fabricate poly-Si NW thin-film transistors (NWTFT) by using sidewall spacer etching technique to define poly-Si NW channels, and the fabricated devices feature a single side-gate structure[2]. Improved characteristics over the planar counterparts, including reduced short channel effects (SCEs) and steeper subthreshold swing, have been observed[3]. However, the ON current of the proposed NW devices is limited by the small conduction width inherent with the single side-gate structure. These issues must be carefully addressed before the NW devices can be inducted to practical application and mass production. In line with this, the adoption of a multiple-gated (MG) structure is promising[4] [5]. The MG configuration is expected to further improve the performance of poly-Si NWTFT devices through an increase in the effective channel width and enhanced gate controllability over the channel. In this work we propose new and simple methods to fabricate MG poly-Si NW devices and investigate the impact of MG on device performance.

2. Device Fabrication

Top layout of the NW devices is shown in Fig. 1. Key steps of the device fabrication are illustrated in Fig. 2, in which the cross-sectional views along the A-B line in Fig.1 in each step are shown. First, TEOS and nitride films were sequentially formed on Si substrates capped with buried oxide (Fig.2(a)). After the patterning of the top nitride layer with an anisotropic plasma etching step, an isotropic wet etching process was used to etch the TEOS oxide layer and form cavities under the SiN layer, as shown in Fig.2(b). Then a 100-nm-thick conformal amorphous-Si layer was deposited, followed by an annealing step performed at 600°C in N_2 ambient for 24 hours to transform the amorphous-Si into poly-Si. Source/drain (S/D) doping was then performed with phosphorus ion implantation (Fig.2(c)). After the generation of S/D PR patterns with a lithographic step, a reactive plasma etching step was performed. Owing to the anisotropic etching process, poly-Si NW channels underneath the nitride hard mask were formed simultaneously during the S/D etching step. Next is the key step to determine the gate configuration: For structure 1 (S1), the nitride hard mask and dummy TOES were retained (Fig.2(d-1)) by skipping the etching process. For structure 2 (S2), the nitride hard mask was selectively removed with a wet etching (Fig.2(d-2)) and the dummy TOES was retained. For structure 3 (S3), both nitride hard mask and dummy TEOS were removed (Fig.2(d-3)). Subsequently, a 20nm-thick TEOS gate oxide and an n^+ poly-Si gate were formed in all devices (Fig.2(e-1) to (e-3)). All fabricated devices then received NH_3 plasma treatment for 2 hour. It should be noted that the three structures which have NW channels of identical shape and size would allow us to investigate and clarify the impacts of MG configurations on device performance as well as the variation of device characteristics. An SEM picture of an S2 NW device is shown in Fig. 3. For comparisons, planar devices with poly-Si channel of 50 nm and gate oxide of 20 nm were also fabricated.

3. Results and Discussion

Figure 4 depicts transfer characteristics of the NW and planar TFT devices with channel length of 2 micron. The drain current is normalized to the channel width. From the figure it is clearly seen that the NW devices show improved performance in terms of steeper subthreshold swing, lower off current, and higher drive current as compared with the planar one. The improvements are attributed to the reduction in the amount of defects contained in the channels with the NW structure. Among the three NW devices, S3 device exhibits the best performance, owing to its enhanced gate controllability with the nearly gate-all-around (GAA) configuration.

To further illustrate the merits of using the NW channels, the transfer characteristics of planar TFTs and S3 NWTFTs of various channel length are shown in Figs. 5 and 6, respectively. Obviously the characteristics of planar devices, including on and off currents, threshold voltage, subthreshold swing, and DIBL, are closely related to the channel length. On the other hand, in Fig, 6 the only parameter showing strong dependence on the channel length is the on current. This indicates the great potential of the NW structure in scaling.

4. Conclusions

In this work, we have proposed and demonstrated a clever scheme to fabricate three types of poly-Si NWTFTs with different gate configurations but identical NW channels, without resorting to advanced lithographic tools. Such scheme allows us to investigate the impact of multiple-gate configuration on the performance of poly-Si NW devices. Our results clearly indicate the dramatic performance improvements made over conventional planar structure with the adoption the NW channels. Moreover, the S3 structure, which has the largest portion of the NW channel surface under effective gate modulation, exhibits the best characteristics among the three types of NW devices.

Acknowledgments

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References

[1] A. G. Lewis, I.-W. Wu, M. Hack, A. Chiang and R. H. Bruce, *IEDM Tech. Dig.*, p.575 (1991).
[2] H. C. Lin et al., *IEEE Electron Device Lett.* (2005) 643.
[3] H. C. Lin et al., *IEEE Trans. Electron Device* (2005) 2471
[4] J. P. Colinge et al., *IEEE Electron Device Lett.* (2006) 120.
[5] D. Hisamoto et al., *IEDM Tech. Dig.*, p.1032 (1998).

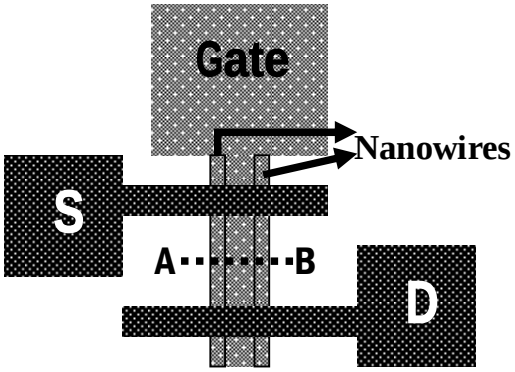

Fig. 1 Top view of the NW-TFT with inverse-T gate and top gate

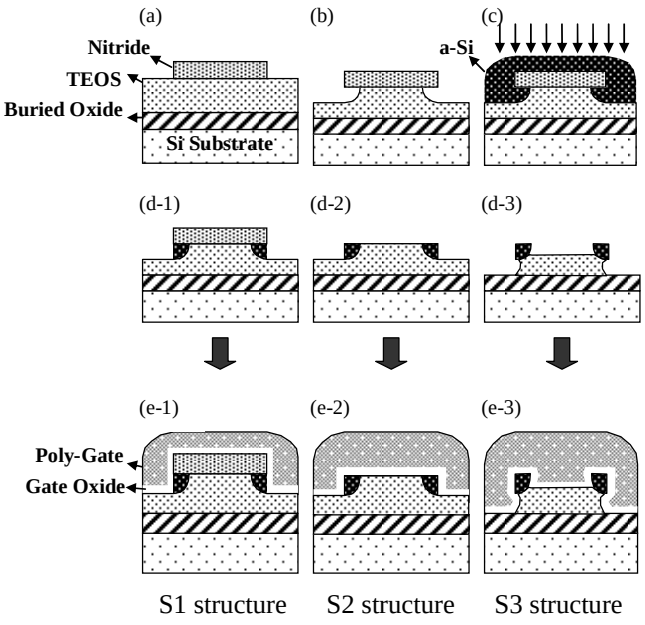

Fig. 2 Process sequence for forming three types of structures.

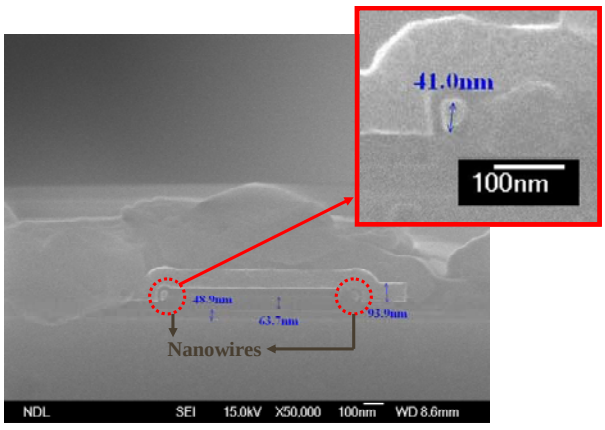

Fig. 3 SEM image of a fabricated S2 NWTFT.

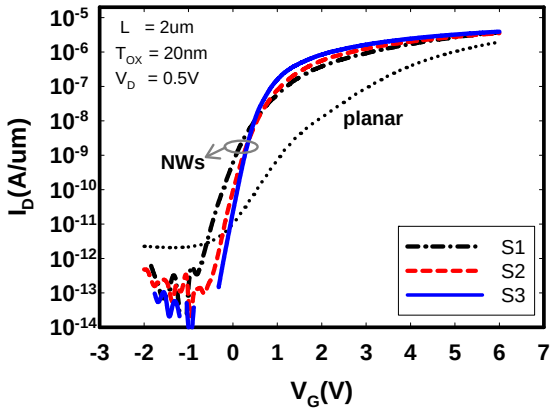

Fig. 4 Transfer characteristics of the planar and NW devices with channel length of 2 micron.

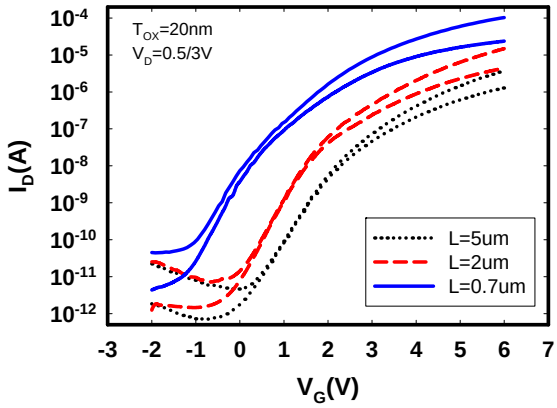

Fig. 5 Transfer characteristics of planar devices with channel length of 5, 2, and 0.7 micron.

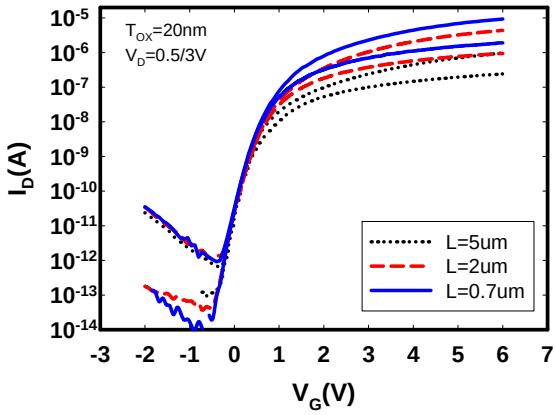

Fig. 6 Transfer characteristics of S3 NW devices with channel length of 5, 2, and 0.7 micron.