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Low-frequency Noise Characteristics of SiGe-channel PMOSFETs with High-compressive ILD-SiN_x Stressing Layer

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1. Introduction

As we continue to aggressively scale transistors in accordance with Moore's Law to nanometer generation, it becomes increasingly difficult to maintain the required device performance. Nowadays, strain-technology was provided an attractive possibility to improve the performance of CMOS transistors. A SiGe-channel PMOSFET technology with high-compressive ILD-SiN_x stressing layer was proposed to enhance hole mobility and improve device current gain [1]. However, its low-frequency noise has not been addressed. In this work, we study the low-frequency noise in SiGe-channel devices with high-compressive SiN_x layer and extract the effective trap density in gate oxide from the noise data.

2. Experiments

The Si- and SiGe-channel PMOSFETs were fabricated using a 90 nm generation technology. The gate oxide thickness was 1.4 nm. The test devices in our work are shown in Fig. 1. To enhance the channel compressive strain, a 1200Å-thick ILD-SiN_x CESL layer was deposited as a high-compressive (-2.0GPa) stressing layer for high-compressive strain device. The low-frequency noise characteristics of PMOSFETs under constant drain voltages (V_{DS} = -0.05V), and various gate voltages (V_{GS}) were measured on-wafer using a BTA9812B noise analyzer.

3. Results and Discussion

The I_D-V_{GS} characteristics and I_D-V_{DS} characteristics are shown in Fig. 2 and Fig. 3, respectively. The SiGe-channel device has higher drain current than Si-channel device due to larger hole mobility. The current can be further improved with high-compressive SiN_x stressing layer. Fig. 4 shows typical input-referred voltage noise spectra (S_{vg}) plotted as gate bias from 10 Hz to 1 kHz for a Si-channel device. The SiGe-channel devices have similar results. All the noise spectra of devices in this work are $1/f^{\alpha}$-like with α in the range of 0.8-1.3. Fig. 5 shows the normalized current noise and $(g_m/I_D)^2$ versus drain current. The $1/I_D$ dependence predicted by Hooge's model is not followed by our data. Whereas, the normalized noise seems to follow $(g_m/I_D)^2$, indicating the noises are dominated by unified carrier number fluctuations.

Figs. 6-8 show the S_{vg} plotted as gate voltage overdrive (V_{GS}-V_T) with different channel lengths at 20 Hz. We found that the high-compressive device has lower noise magnitude at long channel and short channel. On the other words, the S_{vg} is irrespective of strain strength in our PMOSFET devices. It is contrary to the result in previous paper [2]. From the gate leakage characteristics (see Fig .9), it also shows that the high-compressive device has better gate dielectric quality than the devices without high-compressive SiN_x layer. Assuming equal energy direct tunneling of the channel carriers over a rectangular, a trapping time constant is given by

$$\tau = \tau_0 \exp(\gamma x) \quad , \qquad (1)$$

where γ is carrier tunneling coefficient and x is the distance into the oxide from the Si-SiO_2 interface. For the Si-SiO_2 system, the value of γ is typically taken to be 10^8 cm^{-3} and $\tau_0=10^{-10}$ s [3]. Using eq. (1), the trap density corresponding to tunneling depth of 0.6 nm-0.9 nm can be estimated from noise data at f=10 Hz-10kHz.

According to the unified carrier-number fluctuation model [4], we can extract the effective trap density. The extracted effective trap densities at 20 Hz are shown in Tables I-III. The high-compressive strain device has lower trap density, so it has lower low-frequency noise. Besides, the trap density is less dependent on the channel length, so the lower trap density is not due to the strain in channel. Because the incorporated hydrogen species can passivate the interface states of gate oxide when CESL layer was deposited [5], the trap density in high-compressive strain device will decrease.

4. Conclusions

The low-frequency noise characteristics of SiGe-channel PMOSFET with high-compressive SiN_x layer have been investigated. The noise in device with high-compressive layer is lower than that without high-compressive layer. After extracting the trap density, we found the high-compressive strain device has lower trap density and it is less dependent on channel length. Hence, the lower trap density is not due to strain in channel but due to the CESL deposition process.

References

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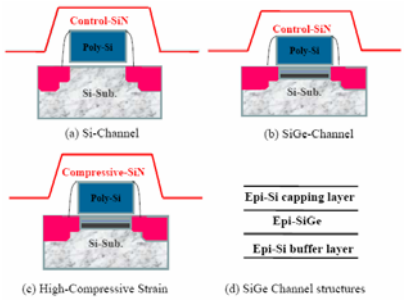

Fig. 1 PMOSFET with Si channel, SiGe channel and high compressive SiN_x layer.

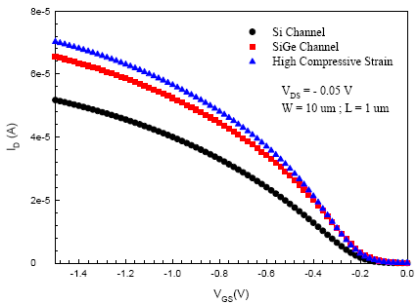

Fig. 2 I_D-V_{GS} characteristics of PMOSFETs.

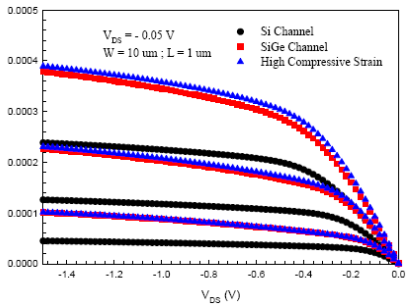

Fig. 3 I_D-V_{DS} characteristics of PMOSFETs.

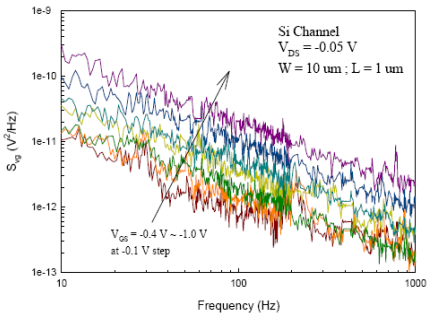

Fig. 4 Input-referred voltage noise spectra versus gate bias from 10 Hz to 1 kHz for a Si-channel PMOSFET.

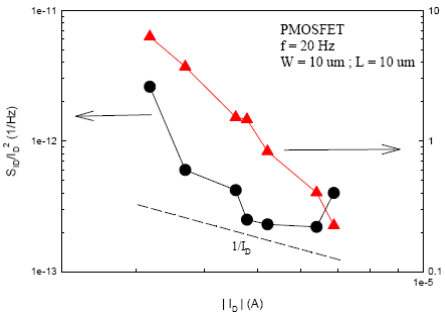

Fig. 5 Normalized current noise spectral density and $(g_m/I_d)^2$ versus drain current.

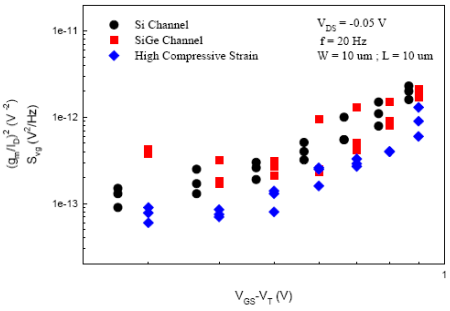

Fig. 6 Input-referred voltage noise versus gate bias at 20 Hz for PMOSFETs with L = 10 um.

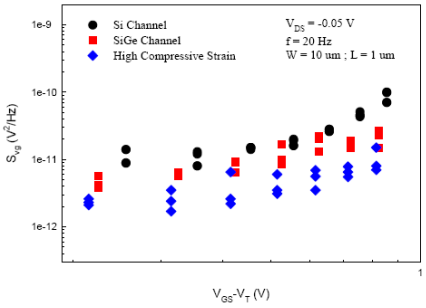

Fig. 7 Input-referred voltage noise versus gate bias at 20 Hz for PMOSFETs with L = 1 um.

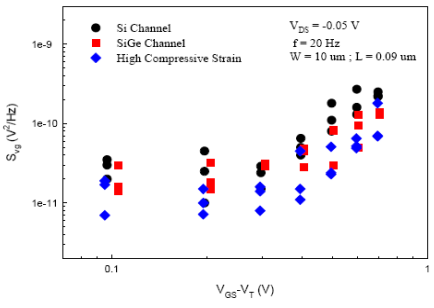

Fig. 8 Input-referred voltage noise versus gate bias at 20 Hz for PMOSFETs with L = 0.09 um.

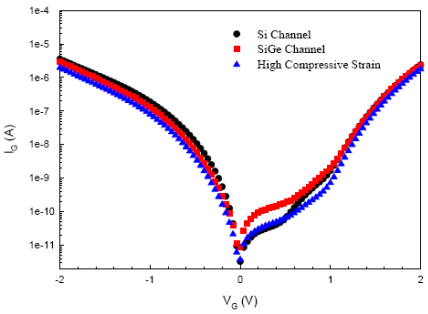

Fig. 9 Gate leakage characteristics of PMOSFETs.

Table I Effective traps density at 20 Hz for PMOSFETs with L = 10 um.

Device (10 um / 10 um)	S_{vg} (V^2/Hz)	N_t ($cm^{-3}eV^{-1}$)
Si-Channel	2.5×10^{-13}	1.15×10^{19}
SiGe-Channel	3.2×10^{-13}	1.47×10^{19}
High Compressive Strain	7.5×10^{-14}	3.44×10^{18}

Table II Effective traps density at 20 Hz for PMOSFETs with L = 1 um.

Device (10 um / 1 um)	S_{vg} (V^2/Hz)	N_t ($cm^{-3}eV^{-1}$)
Si-Channel	1.2×10^{-11}	5.50×10^{19}
SiGe-Channel	6.5×10^{-12}	2.98×10^{19}
High Compressive Strain	1.7×10^{-12}	7.79×10^{18}

Table III Effective traps density at 20 Hz for PMOSFETs with L = 0.09 um.

Device (10 um / 0.09 um)	S_{vg} (V^2/Hz)	N_t ($cm^{-3}eV^{-1}$)
Si-Channel	4.8×10^{-11}	1.86×10^{19}
SiGe-Channel	3.2×10^{-11}	1.32×10^{19}
High Compressive Strain	7.2×10^{-12}	2.97×10^{18}