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Low Power CMOS Stress Degradation Study by Device Current Optimization on SRAM Cell Application

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1. Introduction

One of SoC major application is the low power electronic products in mobile components which low active power and low leakage are the requirements. SRAM cell no doubt to be the most sensitive circuit in system to characterize devices integrated performance. As can be seen in figure 1, enlarge PMOS load transistor Ion can induce better of static noise margin (SNM), also known as read margin. However, tradeoff is needed between write margin and read margin [1]. Fig.2 shows a typical read margin SRAM cell degradation after 1 MHz, 125C, 1.4Vcc, 1000hrs stress. In this work, we present a correlation of N/P MOS Ion ratio with stress degradation and propose an empirical model of SRAM read speed degradation in terms of power low of Vccmin drifting by shmoo characterization.

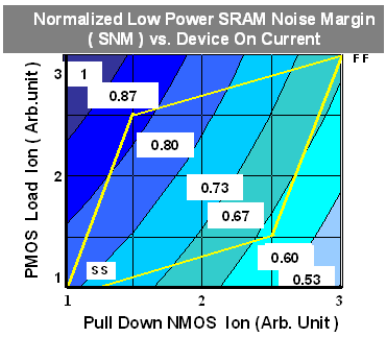


Fig.1 Normalized Static noise margin (SNM)

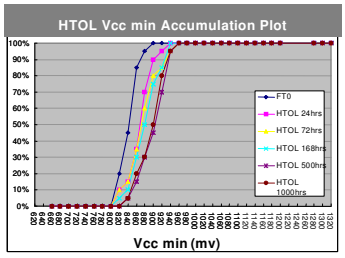


Fig.2 SRAM Vccmin drift after 125C, 1000hrs stress

2. Experiments

65nm low power CMOS with typical 1.2volt Vcc devices were fabricated to form 6T-SRAM and its Vccmin drift are investigated by the index of alpha ratio (the ratio of PMOS load transistor Ion to NMOS pass gate transistor Ion). Vccmin drift after stress has been correlated to PMOS NBTI effect [2] [3], further study on alpha ratio correlation is presented in this works. Fig.3 reveals less hot of PMOS (less Ion, lower alpha ratio) can have more Vccmin drift (~ $t^{0.16}$) by NBTI effect which compared to higher alpha ratio of SRAM cell.

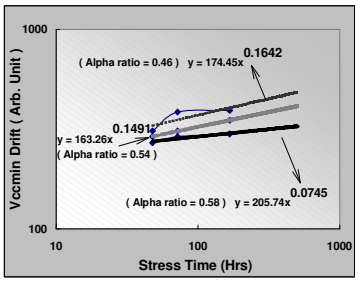


Fig.3 Vccmin drift with time dependence on different alpha ratio (0.46, 0.54, 0.58).

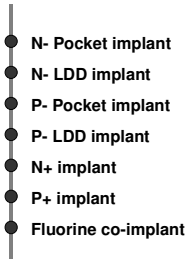


Fig.4 Fluorine co-implant process flow

Fluorine co-implant is reported to improve FEoL reliability [4], used process flow is shown in Fig.4. The Fig.5 compares Vccmin drift accumulation plot including with and without Fluorine co-implant on alpha ratio around 0.54. It show reverse trend compared to figure 2 that Vccmin drift after 1000hrs stress toward lower Vccmin value which can be attributed to the increasing of PMOS Ion. Fluorine co-implant devices reveal tighter Vccmin distribution after stress (Fig.5b) than non Fluorine incorporation (Fig.5a). Fig.6 is the 50% accumulation result from Fig.5 with other alpha ratio splits. With Fluorine co-implant devices perform less of Vccmin drift than that of without Fluorine under alpha ratio range from 0.4 to 0.55. It had been reported that the incorporation of Fluorine on silicon interface causes some silicon strain release and result in better reliability degradation immunity. Fig.7 is the proposed model of Fluorine incorporation by view of energy band concept. The silicon and fluorine bonds can reduce the hydrogen diffuse when NBTI effect is triggered.

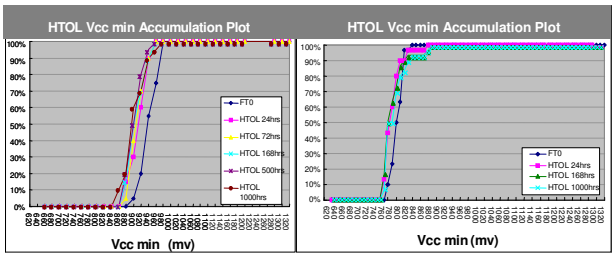


Fig.5 Vccmin drift accumulation plot (5a_left : without Fluorine co-implant) (5b_right : with Fluorine co-implant)

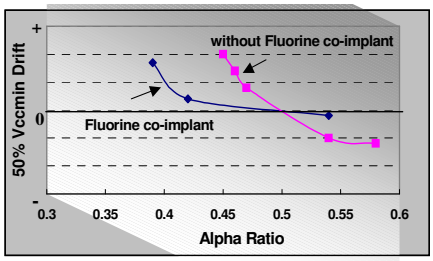


Fig.6 50% Vccmin drift comparison on Fluorine co-implant

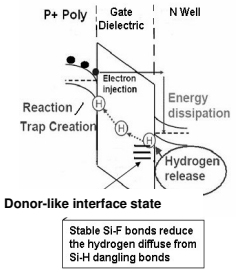


Fig.7 Energy band diagram of PMOS NBTI effect on Fluorine co-implant

Vccmin shmoo plots are investigated on Fluorine co-implant devices. Fig.8 reveals that SRAM balance status on Vdd with Vcell decays as defined by increased Vccmin after stress.

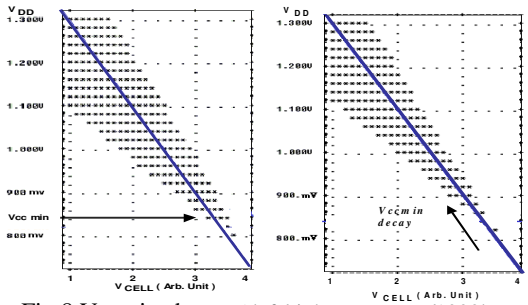


Fig.8 Vccmin shmoo (left/right:non-stress/1000hrs stress)

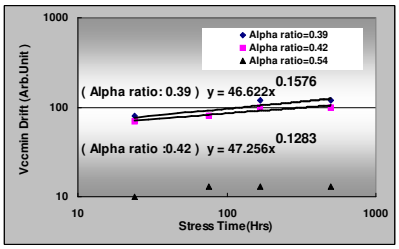
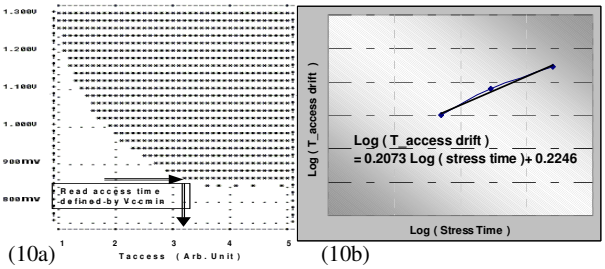
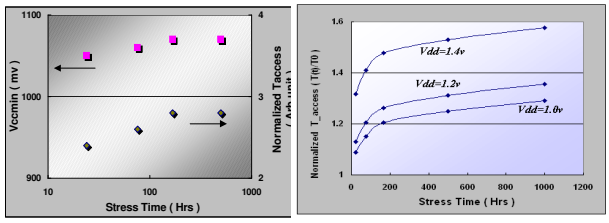


Fig.9 Vccmin drift with time dependence on alpha ratio split

Fig.9 shows Vccmin drift time dependence from shmoo data which indicates less hot of PMOS (lower of alpha ratio:0.42) perform better NBTI immunity than non Fluorine co-implant devices.(compared to Fig.3, alpha ratio :0.46)



(10a) (10b)



(10c) (10d)

Fig.10 (a)Shmoo plot of access time defined by Vccmin; (b) Degradation follow power low;(c)Correlation for access time and Vccmin(d)access time drift simulation with Vdd split.

SRAM read access time is analyzed by shmoo point of view as Fig.10(a) which the speed limitation of read mode on Vccmin can be further modeled by inverter timing delay concept. Fig.10(b) show the stress degradation of access timing drift which the power low exponent is 0.20. Correlation on Fig.10(c) indicates stress degradation is similar on Vccmin drift and access time drift. According to the empirical expression on inverter delay, it can be further proposed access timing stress degradation model as Eq.(1). This can be used to predict speed degradation shown in Fig.10(d) .

$$\text{T\_access (stress time)} \propto V_{DD}\left[\frac{1}{V_{DD} - Vt_0 - \Delta Vcc\ min} - \frac{1}{V_{DD} - Vt_0}\right] \quad (1)$$

3. Conclusions

SRAM Vccmin degradation behavior by SRAM cell alpha ratio is shown in this paper. 50% accumulation plot of Vccmin drift indicates less shifting after stress on the Fluorine co-implant devices. It can be attributed to better Vccmin window by shmoo plot characterization. SRAM read access timing drift shows strong correlated to the Vccmin drift after high temperature stress. Besides, access timing stress degradation model also is presented in this works.

References

[1] Kunhyuk Kang et al., IEEE ITC. 11.1 (2007).
[2] Sanjay V. Kumar et al., IEEE ISQED. (2006) .
[3] S.Chakravarthi et al., IEEE IRPS. (2004) 273.
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