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# A Vertical-Channel Metal-Oxide-Semiconductor Field-Effect Transistor with Fully-Oxidized Silicon Beam Isolation

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## 1. Introduction

In response to ceaseless requirement for higher performance of large-scale integrated circuits, planar metal-oxide-semiconductor field-effect transistor (MOSFET) has been continually shrunk since 1970. Even if its performance has been improved dramatically, various kinds of adverse effects, such as short-channel effect and increased difficulty in patterning, have appeared. To reduce these effects, vertical-channel transistors have been proposed [1, 2] in the past.

This work proposes a novel vertical-channel pillar-type MOSFET with a novel isolation structure. The technique utilizes conventional local oxidation of silicon (LOCOS) technique resulting in pillar transistors which are seperated by LOCOS field oxide each other, as shown in Fig. 1.

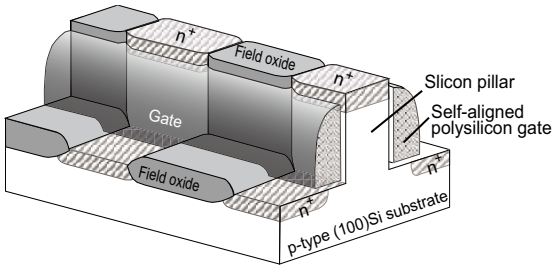


Fig. 1 Proposed vertical silicon pillar MOSFET's isolated with field oxides which are obtained by full oxidation of silicon beam.

Since field isolation regions are formed by the oxidation of one straight silicon beam, all vertical silicon pillars are physically connected each other. When misalignment of the gate to the pillar is $F/2$, the proposed device does not suffer from the misalignment, as shown in Fig. 2.

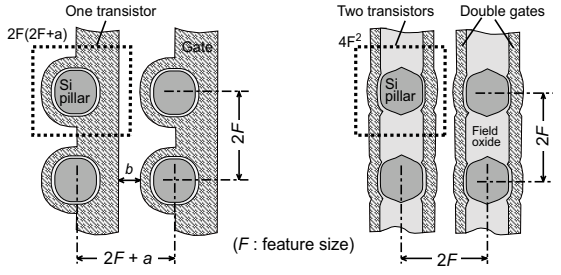


Fig. 2 Gate misalignment to the pillar by $F/2$ requires wider spacing of $2F+a$ for the conventional (a), but does not for the proposed (b).

## 2. Sample preparation

A process sequence to realize the proposed device is shown in Fig. 3 featuring LOCOS process execution and self-aligned gate formation.

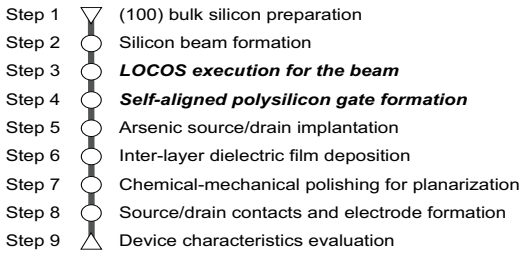


Fig. 3 A process sequence to realize the proposed device.

Devices are fabricated on p-type, (100)-oriented, 8-12 Ω-cm, and 50 mm$^{\phi}$ silicon substrate. Initial beam height is 300 nm. Gate oxide thickensses are 7.3 nm on (110) sidewall and 4.3 nm on (100) surface.

Field oxide transformed from the beam and residual polysilicon gate after the process step 4 are shown in Fig. 4. A top plane view of the structure is shown in Fig. 5. Note that the width of the LOCOS field oxide is close to that of silicon pillar. Even though the thickness of the initial LOCOS field oxide is about twice as much as that of the silicon beam, controlled etching of the oxide realized almost the same thickness.

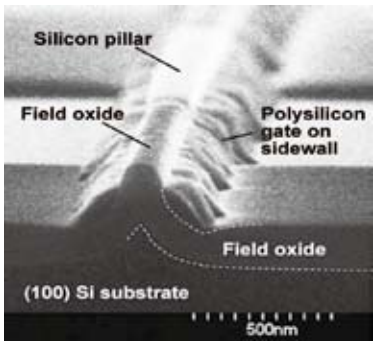


Fig. 4 An SEM cross-section of the proposed device at a process sequence of step 4.

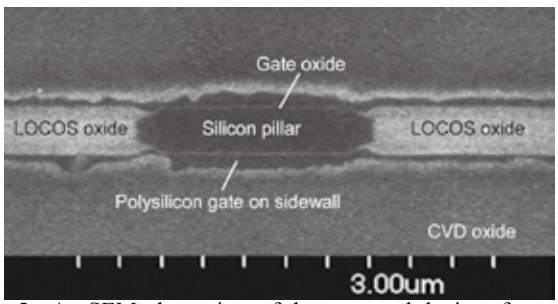


Fig. 5 An SEM plane view of the proposed device after process execution of step 4. Since chemical-mechanical polishing is not sufficient enough, only top portion of the polysilicon gate appears.

## 3. Electrical Characteristics

A measurement setup is shown in Fig. 6. The $n^+$ region of the top of the pillar works as common drain for two transistors in a pillar.

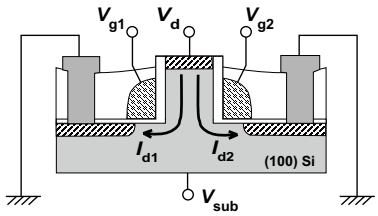


Fig. 6 Measurement setup. Source length is 5 μm causing a transconductance degradation to some extent. Total length of L-shaped channel, $L_{total}$ is 250 nm. Beam width is 300 nm.

$I_d$-$V_g$ characteristics in log and liner scales are shown in Figs. 7 and 8, respectively. Since drain currents of $I_{d1}$ and $I_{d2}$ can be controlled seperately, one silicon pillar definitely works as seperate two transistors when the top $n^+$ region is divided into two parts with additional process.

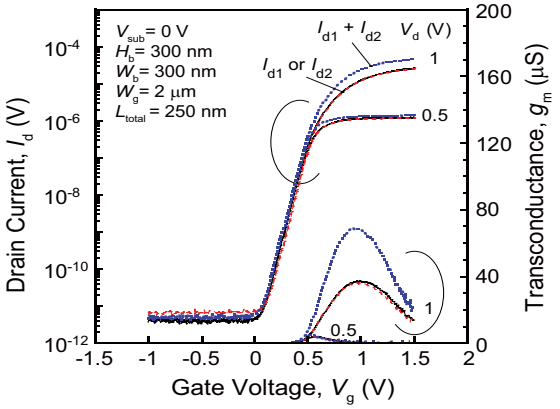


Fig. 7 $I_d$-$V_g$ characteristics in log scale. Beam height, $H_b$, beam width, $W_b$, channel width, $W_g$, and L-shaped total channel length, $L_{total}$ are 300 nm, 300 nm, 2 μm, and 250 nm, respectively.

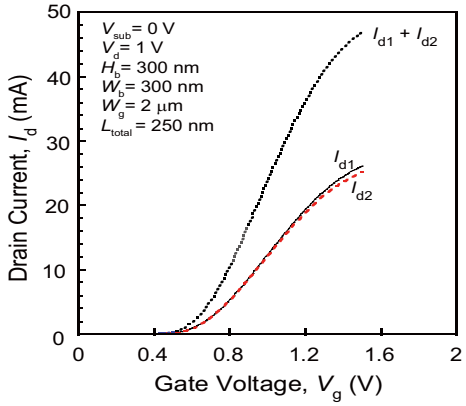


Fig. 8 $I_d$-$V_g$ characteristics in linear scale.

$I_d$-$V_d$ characteristics are shown in Fig. 9. A drain voltage offset of about 0.5 V is well attributed to accidentally formed drain-to-gate offset. It is evident form the fact that transistor configuration with $n^+$-top source does not work adequately.

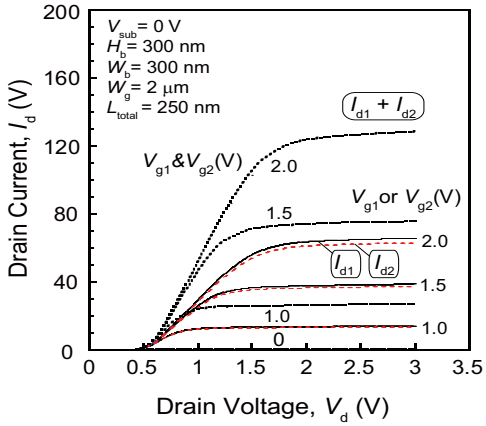


Fig. 9 $I_d$-$V_d$ characteristics.

A substrate voltage dependence of $I_d$ is shown in Fig. 10. This shows substrate is normally formed in these device structures even with 300-nm thick silicon beam.

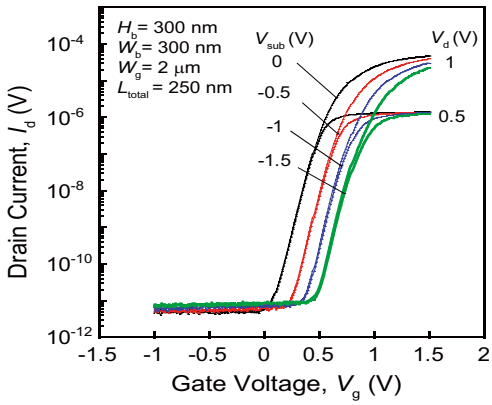


Fig. 10 Sustrate bias dependence of drain current.

## 4. Conclusion

A novel vertical MOSFET with a novel isolation technique is proposed. Since isolation region is formed as a part of silicon beam by LOCOS technique, transistor's active regions and field oxide isolation regions are physically connected resulting in self-aligned gate formation. Furthermore, both straight-line etching patterns of the beam and LOCOS can avoid very critical tiny-dot patterning in conventional stand-alone pillar transistors.

Obtained electrical characteristics are satisfactory in general except some performance due to accidentally formed gate-to-drain offset. Two seperate transistors in a pillar has a strong potential to realize $2F^2$ memory cell such as DRAM, EEPROM, etc. Thus the proposed vertical-channel MOSFET with fully-oxidized silicon beam isolation is very promising for ulta-high density transistors and memories.

### References


[1] W. F. Richardson, D. M. Bordelon, G. P. Pollack, A. H. Shah, S. D. S. Malhi, H. Shichijo, S. K. Banerjee, M. Elahy, R. H. Womack, C. Wang, J. Gallia, H. E. Davis, and P. K. Chatterjee, Internat. Electron Devices Meet. Tech Dig. (1985) 714.

[2] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, Internat. Electron Devices Meet. Tech Dig. (1988) 222.