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Layout Dependence of SiGe Strain Effect and STI Induced Defects in 45nm p-PMOSFETs with Strain SiGe Source/Drain

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I. Abstract

The influence of the mechanical stress induced by both strained SiGe source/drain(S/D) and shallow trench isolation (STI) on interface states in 45 nm p-PMOSFETs were studied in details. An improved low gate-leakage gated-diode measurement (L^2-GD) was applied to investigate the total induced defects. As the channel length scales to less than 0.24 μm, the total defect density reduces with decreasing the channel width remarkably as opposed to the increase in the conventional deep submicron devices.

II. Introduction

The defects resulted from the STI mechanical stress are recently identified as the cause of anomalous off-state leakage current [1-2]. The mechanical stress issue will be more significantly in the next-generation nano-scale CMOS technologies for the channel is gotten closer to the STI edge by the continuously shrank active area.. On the other hand, the strain engineering such as SiGe S/D [3-4] has been widely applied to improve device mobility for the advanced high speed and low power CMOS devices. However, the strain engineering also creates a large number of acceptor-like interface states (Nit) at the gate oxide/extension of S/D interface [5], and thus affects other reliability issues. In the past, strain engineering worsens the hot carrier reliability and NBTI (negative bias temperature instability) in CMOSFET have been reported [6-7]. Nevertheless, so far, the effect of SiGe S/D strain on STI caused degradations has not been reported.

In this paper, we investigate the layout dependence of defects resulted from SiGe and STI strain in 45nm devices with and without strain SiGe S/D by both measurement and simulation. Owing to the larger leakage caused by the ultra-thin gate oxide thickness (less than 2 nm) and smaller dimension (width/length less than 1μm /0.06μm) of the device, the conventional charge pumping method is not suitable to get the exact interface traps and oxide charges. Therefore, in this work, we use the improved L^2-GD measurement to investigate the effect of the SiGe and STI stress on the defect density [8]. It is found, for a SiGe S/D deep nano-device, the total defect density decreases with decreasing the channel width for the length less than 0.24 μm. For the short length and width in SiGe devices, the channel stress will be changed from the pure SiGe and STI uniaxial strain (parallel to the channel) to the combination of SiGe, STI and edge-STI strain. In other words, the SiGe strain will be relieved by the edge-STI stress. This is different to the conventional devices, and the mechanism has been explained well with a proposed model. This work promises exploration of mechanical stress issues in future nano-scale devices and circuits.

III. Device Fabrication and Measurements

The p-MOSFET devices were fabricated by a state-of-the-art 45-nm CMOS foundry technology. After STI and gate formation, the in-situ boron doped p+ $Si_{0.8}Ge_{0.2}$ S/D with boron concentration was selectively deposited. The gate was boron doped P+ poly silicon with a 1.6~1.7nm nitride oxide grown. Subsequently, processes of LDD implant, spacer formation, post implantation RTA annealing, and back-end processes were implemented to complete the devices. More process details could be found in the reported literature [5,7]. For comparison purpose, devices without SiGe S/D were also fabricated under the same processing conditions. We studied transistors of various width/length (as shown in Fig. 1.) combinations to investigate the dependence of the device interface states. We adopted the L^2-GD to measure the interface defects and location in gate oxide [8]. In the L^2-GD measurement, shown as the Fig. 2, the drain current was examined under sweeping gate voltage of –1 to 4V by fixing drain node under 0.3V and floating source node, respectively. In Fig. 3, we could find that the third peak was most obvious, and we propose the third peak (Igd^{3rd}_max) to use an index of gate oxide damage quality because the gate oxide is weakest near the S/D extension region.

IV. Results and Simulation

Without SiGe S/D strain, Igd currents are higher with larger widths. It is obvious that the oxide gets more interface defects with increasing width (active region is also increased) in non-SiGe samples as shown in Fig. 4. However, when we modify the Igd current by changing width as shown in the Fig. 5, we find that the Nit is not affected by different widths. They merge in a line, and the Igd currents are higher when lengths get narrower because the STI (compressive stress) is closer to the channel center with decreasing length, and results in larger stress to produce defects [9]. With SiGe in S/D cases, as shown in Fig. 6, the behaviors are different. When length is long enough, the device with SiGe S/D gets more oxide interface states than that of the non-SiGe one. However, the defects start to degrade as length becomes shorter. Especially, as length is less than 0.24 um, Nit decreased more serious from width = 10 to 0.3 um. As the Fig. 7 showed, because the edge-STI limited the SiGe strain for small width sample, it is the reason why with SiGe strain the interface states would not increase with decreasing length in the narrower width samples. For the shrot length and width in SiGe devices, the channel stress will be changed from the pure SiGe and STI strain to the combination of SiGe, STI and edge-STI strain. In three-dimensional solids, a compressive strain in one direction produces tensile strain in the other two directions, this is called Possion's effect and can be estimated using Poisson's ratio γ. For cubic material such as silicon, Poission's effect in all directions can be described by a single number γ, which is 0.28 [10]. The uniaxial SiGe transverse tensile stress is balanced by edge-STI stress, and it also affects the SiGe longitudinal compressive stress. In state-of-the-art integrated circuit designs, the majority of PMOS transistors are in the width 1um and beyond, which is the region where the stress from SiGe and STI is most sensitive to changes in device width.

Stress distribution near the S/D extension region with various lengths is extracted by T-CAD simulations, as shown in the left insert of Fig. 3. The expansion of SiGe causes compressive stress along channel (Sxx) direction (Fig. 8), and has the maximum stress near the S/D LDD extension region far from 0.02 μm to the channel center (for length=0.06μm). Besides, as the length scales down to 0.06μm, the simulation results show the stress near the S/D LDD region is decreased, as shown in Fig. 9. The Igd density (defects) is consistent with the simulation stress in the channel direction. Due to the constraint from edge-STI stress, the longitudinal stress (Sxx) will no longer continuously increase with the channel length decreasing infinitely.

IV. Conclusions

The effect of narrow width and length on the interface defect density was investigated with the improved low gate-leakage gated-diode (L2-GD) measurements in details. We find that for SiGe S/D device, as the channel length less than 0.24μm, the compressive stress (Sxx) induced by the SiGe S/D region and STI do not increase with decreasing length. Simultaneously, the compressive stress is limited by the edge STI more significantly, thus leading to the defect density decreases much more at narrower width. This is different to

the conventional non-SiGe device; the stress enhanced by the scaled width and length further strains the gate oxide, thus generating more interface states.

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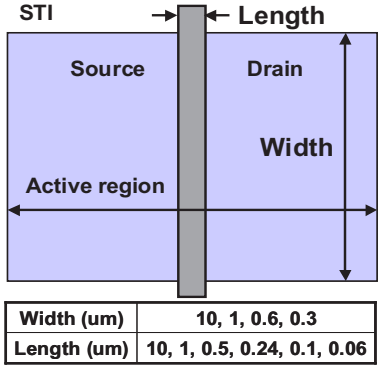

Width (um)	10, 1, 0.6, 0.3
Length (um)	10, 1, 0.5, 0.24, 0.1, 0.06

Fig.1 shows the schematic view of the device geometry effects changed by width and length.

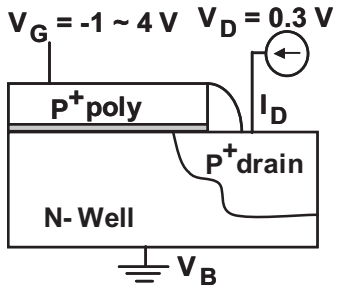

Fig.2 shows the cross-section of the L^2-GD method.

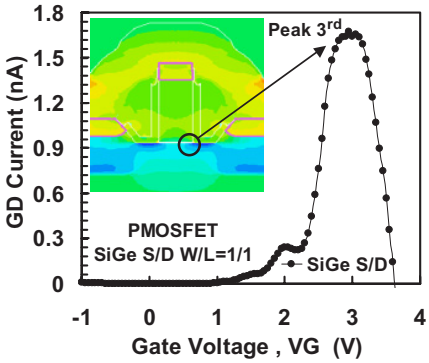

Fig. 3 shows gated-diode current measurement of SiGe S/D. The 3rd peak (in LDD extension region) is most obvious

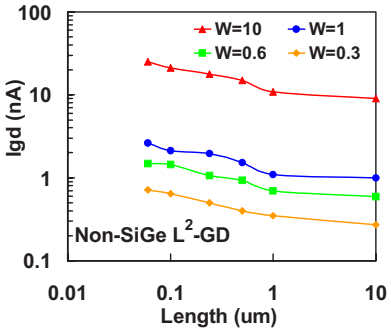

Fig.4: The Igd values of non-SiGe in 3rd peak are plotted as function of length, and shown in different width.

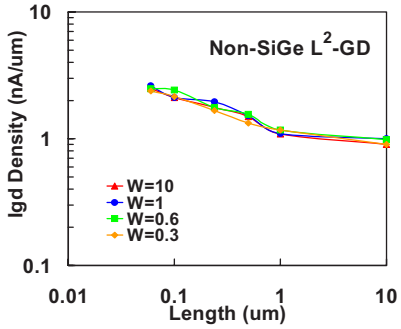

Fig.5: The Igd density values of non-SiGe modified by width from Fig. 4 are plotted as function of length, and shown in different width.

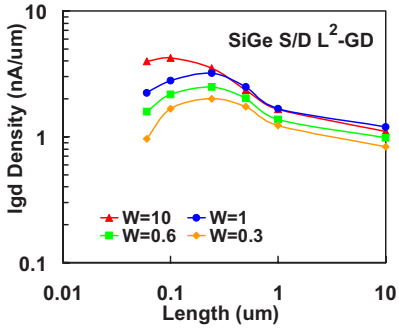

Fig.6: The Igd density values of SiGe S/D modified by width are plotted as function of length, and shown in different width.

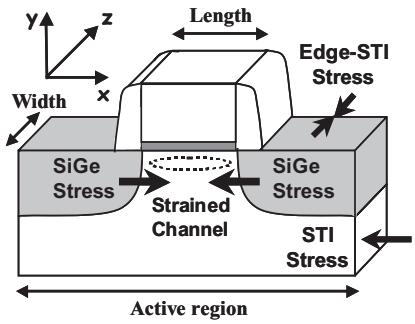

Fig.7 shows the stress factors of SiGe S/D, STI, and edge-STI.

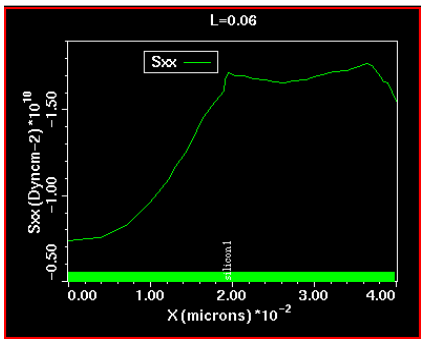

Fig.8: The maximum lateral stress (Sxx, 5um far from the channel surface) is near the S/D extension region.

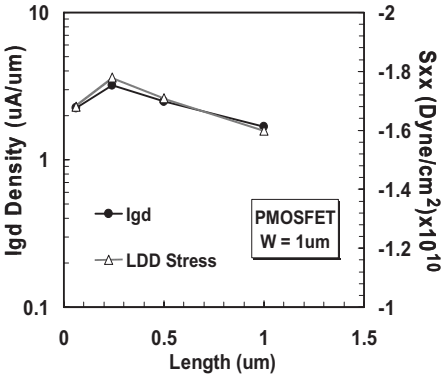

Fig.9: The SiGe Igd density modified width and channel stress is plotted as function of length.