NROM Retention with Distributive Cycling Stresses

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I. Introduction

A promising flash memory NROM [1] based on localized charge storage in nitride layer have been proposed in recent years (Fig. 1a). We have studied the NROM charge retention affected by relaxation effect and vertical charge redistribution for distributed delays and gate bias during cycling stresses. The relaxation effects in cycling [2] can recover some program and erase damages for the bottom oxide and effectively improve the charge retention (Fig. 1b) in high temperature. Furthermore, a variety of relaxation conditions with different cycling distribution and their retention characteristics are also studied. Then, a new NROM retention model has been developed for the lifetime prediction with different distributed cycling stresses. Besides, a new operation sequence for NROM cell, Two-Step Erase Cycling (TSEC) stress, with additional gate bias after erase is proposed for NROM retention further improvement. This new cycling scheme can change the charge distribution of NROM cell, a shrinking threshold voltage shift is therefore obtained at high temperature retention.

II. Experimental and Operational Scheme

The experimental 0.1um NROM cell was fabricated with channel width/length by 0.25um/0.25um. The cycle conditions for program are $Vg/Vd/time = 8V/3V/100\mu sec$ and for erase are Vg/Vd/time = -5.5V/5V/10msec. Reverse read method is applied for wide on/off window. For characterizing the cycling recovery effect in adding certain relaxation time during cycles, different operation procedures are performed to compare and quantify the relaxation magnitude after baking. In order to improve the NROM retention by uniform charge distribution in nitride layer, an extra positive gate pulse right after erase operation is implemented to affect the electron and hole locations after erase, which is named as two-step erase cycling (TSEC) flow as illustrated in Fig.2 [3]. Furthermore, a two dimensional simulation is used to explain the characterization results and investigate the effect of charge re-distribution in nitride layer, and then to elucidate the retention improvement with the new cycling conditions.

III. Results and Discussions

An obvious relaxation effect of NROM cell has been observed and shown in Fig. 3, where 10K (10000) cycling has different relaxation arrangements: no relaxation, insert 10sec relaxations between every 1,000 or 100 cycles. Except the cell without relaxation, the other two cells with relaxation perform similar cycling recovery effect after 720hrs post-cycled bake at 125° C. It clearly shows that, although the cells with and without relaxation have all been stressed through same 10K cycles with similar initial threshold voltage before bake, the cell with relaxation (dash line) shows much less threshold voltage shift after bake than the cell without relaxation (solid line). Thus, the retention reliability of NROM cell is not only affected by the number of cycling stresses, but also influenced by the procedure and method of cycling stresses. Besides, considering the temperature effect of the new retention dominant factor, we performed these distributive cycling sequences at different baking temperatures $(25^{\circ}C, 85^{\circ}C \text{ and } 125^{\circ}C)$ for characterizing the charge loss and the result is summarized as Fig. 4. In order to quantify the thermal excitation including the new factor of cycling relaxations, a new empirical equation [4] is excerpted to model the new retention factor with various distributive cycling stresses. The main equations are listed as below:

$$\Delta \mathbf{V}_{t} = \Delta \mathbf{V}_{t,\text{SAT}} \cdot \{1 - \exp[-(t/\tau)^{\beta}]\}$$
(1)

$$\tau = \tau_{o} \cdot \exp[E_{a} / kT]$$
⁽²⁾

$$\beta = T / T_{o}$$
(3)

According to the Meyer Neldel compensation rule [5]:

$$\tau_{o} = \tau_{\infty} \cdot \exp[-(E_{a} / E_{MN})]$$
(4)

Table 1 shows the parameters of the three cycling conditions and the activation energy (Ea) further provide an accurate lifetime prediction for the cell with distributive cycling sequences, which is much closer to user's operational custom than the previous model considering continuous cycling only. Moreover, a new Two-Step Erase Cycling (TSEC) is introduced to prolong the retention time as shown in Fig. 5. The new method can provide better retention reliability by creating more uniform charge distribution in nitride layer. Fig.6 shows the retention behavior of the distributive two-step erases in 1000 cycling with post-cycled baking at different temperatures. Comparing the post-cycled bakes with different gate pulses is shown in Fig.7. It plainly exhibits that the threshold voltage deviation is reduced for the gate pulse ranging from 6V to 8V. The according simulation result is shown in Fig.9 to illustrate the effect of charge re-distribution. The uniform distribution in nitride layer can be achieved by proper additional gate pulses in erase operation.

IV. Conclusion

The relaxation effect and vertical charge redistribution can significantly improve the charge loss of NROM cell. The additional time delays during cycling can provide the crucial rest time for recovering the stress induced oxide traps, a superior retention is therefore achieved. Furthermore, a new cycling scheme, TSEC operation, with more uniform charge distribution is also used to reduce the electrical field in nitride and improve the retention for high density memory application.

Reference

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Fig. 2(a) The Two-Step Erase Cycling (TSEC) flow with (b) the program /

Fig. 1(a) Cross-section of NROM cell. (b) Illustration of 10K distributive cycling and post-cycled baking.



Fig. 3 Threshold voltage shift after 10K cycling for post-cycled bake at 125°C.



Fig. 4(c) Post-cycling retention with 10sec relaxations between 100 to 100 cycles.



Fig. 6 10K TSEC retention at different post-cycled baking temperatures.



erase timing diagram.

Fig. 4(a) Post-cycling retention without relaxation in cycling.



Table 1 Retention model parameters with the consideration of relaxation effects



Fig. 7 TSEC with different gate pulses retention after 10K cycling post-bake at 125°C.

10 100 Bake Time (hr) Fig. 5 Retention of NROM relaxation and TSEC with different intervals between 10K cycles for post-cycled bake at 125°C.

1000



Fig. 8 Id-Vg simulation curves for various charge distributions in nitride layer.



Fig. 4(b) Post cycling retention with 10sec relaxations between 1K to 1K cycles .

