

## A Dual-Gate Memory Cell with Two Inter-poly Oxides

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### 1. Introduction

This paper presents a new memory concept with dual-gate and two different inter-poly oxides. This new application allows a high density EEPROM memory and a cell programming only with the dual-gate without high bias on drain or source. On a previous work [1], a dual-gate structure was used to perform the memory operations without select transistor which allows, compared to standard EEPROM, to shrink the cell and to improve its lifetime [2-3]. Moreover, without high drain potential during writing operation, we eliminate leakage current due to Band To Band Tunneling (BTBT) and also its hot holes injection generated through the tunnel oxide which can degrade cell reliability [4-5].

### 2. The dual-gate with two inter-poly oxides memory concept

The memory cell concept is to use two different ways of charge injection during erasing and writing operations due to dual-gate. A schematic cross-section of this new cell is shown in Fig.1.

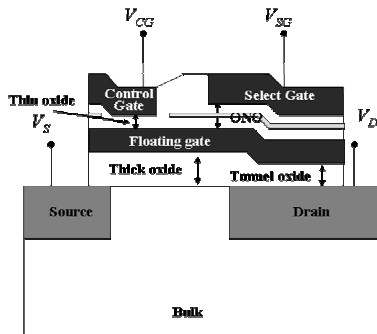


Fig.1 A schematic cross-section of the new transistor.

Above the floating gate, the second poly-silicon layer is used for the two gates. The control gate ( $V_{CG}$ ) is separated from the floating gate by 6nm inter-poly oxide whereas select gate ( $V_{SG}$ ) is separated by 15nm ONO inter-poly isolation. The first oxide level is composed with thin tunnel oxide (<10nm) upper the drain area and a thick oxide (20nm). The cell is programmed by Fowler-Nordheim mechanisms. For erasing operation, we applied a high signal on  $V_{CG}$  and  $V_{SG}$  in order to inject electrons into the floating gate (Fig.2 on the left). For writing operation, we applied a high signal on  $V_{CG}$  to remove electrons from the floating gate to the control gate (Fig.2 on the right).

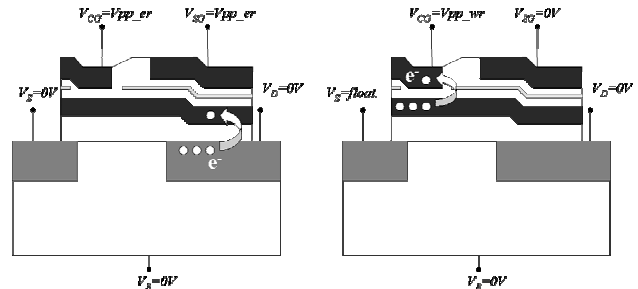


Fig.2 Erase (on left side) and Write (on right side) operations.

In read mode,  $V_{CG}$ , source ( $V_S$ ) and bulk ( $V_B$ ) are grounded, a constant potential is applied on drain ( $V_D$ ) and we read the drain current  $I_D$  versus  $V_{SG}$ . The cell memory matrix is described on Fig.3. Table I resumes the different potentials to program cell A without programming the other cells.

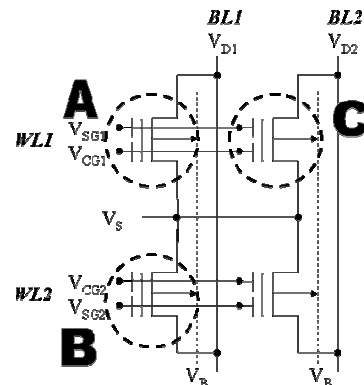


Fig.3 Memory matrix.

Table I Summary for memory operations.

Cell B and C are unselected.

Electrodes	Write cell A	Erase cell A	Read cell A
$V_{CG1}$	10V	12V	0
$V_{CG2}$	0	0	0
$V_{SG1}$	0	12V	Vread
$V_{SG2}$	0	0	Voff = -4V
$V_{D1}$	0	0	0.8V
$V_{D2}$	10V	4V	0

The memory matrix must be written by word and erased by bit in order to control correctly the memory array. If we program the array by bit, in write mode we have to inhibit the cells on the same word line by applying a high potential on the bit lines (Table I) and so we induce an unneeded stress.

### 3. Electrical results

#### Static results

The electrical results provides from a  $0.67\mu\text{m}^2$  cell prototype designed in a  $0.13\mu\text{m}$  technology (Fig.4).

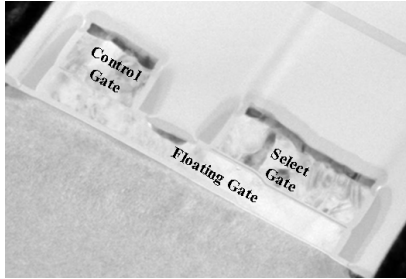


Fig.4 XSEM of this new memory cell.

Static electrical results are presented in Fig.5. These results are compared to compact model simulations.

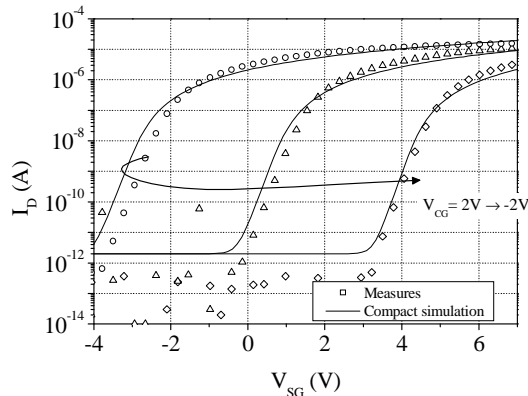


Fig.5 Static  $I_D$ - $V_{SG}$  characteristic for different  $V_{CG}$  polarizations (measures compared with compact simulations).

In static mode, we apply a constant potential on  $V_{CG}$ , to control "virtually" the value of the threshold voltage ( $V_{TH}$ ), and we measure drain current versus  $V_{SG}$  potential. Fig.5 shows  $I_{DS}(V_{SG})$  current measurement and simulation for several  $V_{CG}$  potentials. A variation of 2V on the fix potential  $V_{CG}$  produces a shift of 3.5V on  $V_{TH}$  of the transistor. The same operation with applying the constant potential on  $V_{SG}$  shows the impact of the two gates on the coupling ratio. These static electrical results bring to light a particular functionality of the cell which is the possibility to adjust the threshold voltage  $V_{TH}$  of the transistor. We can notice on Fig.5 a good correlation between the electrical compact model simulations and electrical measures.

#### Dynamic results

With a 12V erase pulse and a 9.8V write pulse, the programming window at  $1\mu\text{A}$  is about 4V (Fig.6). The write efficiency can be increased by applying an additional negative potential on  $V_{SG}$ . The difference between measures and simulations in the subthreshold region are due to the interface traps which are not yet include in the compact model.

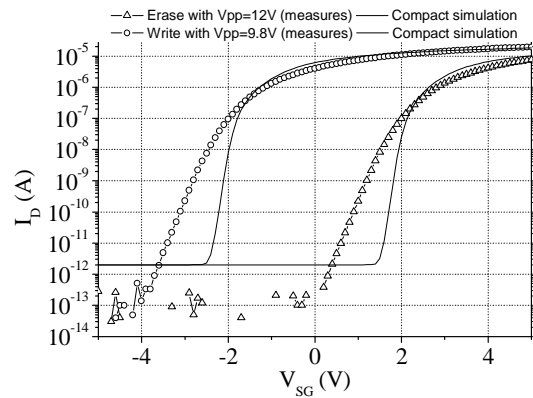


Fig.6  $I_D$ - $V_{SG}$  characteristics depicting the programming window.

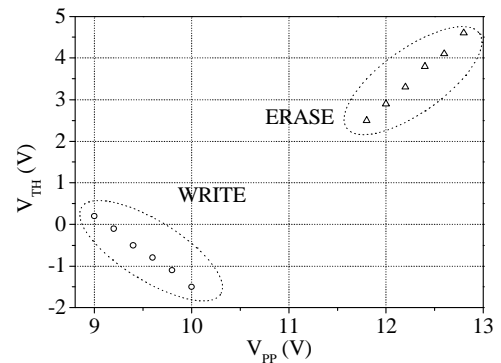


Fig.7  $V_{TH}$  variation versus programming potentials (read at  $1\mu\text{A}$ ).

Fig.7 resumes  $V_{TH}$  variation in function of the applied potentials for programming the cell. The read conditions must be control in order to eliminate possible read disturb of the cell. According to Fig.7, this  $0.67\mu\text{m}^2$  cell has a good functionality with programming potentials close to those of standard EEPROM but with a smaller cell area. Moreover the programming mechanisms used two different ways so we can suppose decreasing the oxides degradation.

### 4. Conclusions

In conclusion, the dual-gate cell with two inter-poly oxides allows a high density of integration compared to standard EEPROM. A first  $0.67\mu\text{m}^2$  cell prototype shows a good functionality with a programming window of 4V, by applying only high potentials on the two gates to eliminate BTBT due to drain bias. Compared to STMicroelectronics standard EEPROM, the cell size is reduced by 48%. Moreover the new cell has two ways of charge injections (through the tunnel oxide and the inter-poly oxide between floating gate and control gate) contrary to standard EEPROM which is programmed only through the tunnel oxide. Thus we should attenuate tunnel oxide degradation.

### References

- [1] J.R. Raguette et al., *ISDRS 2007*, 12-14 Dec. 2007.
- [2] W.D. Brown, J.E. Brewer, IEEE press, 1998.
- [3] K. Hieda et al., *IEEE Trans. Electron Devices*, Volume ED-32, n°9, pp. 1776-1780, 1985
- [4] R. Laffont et al., *IEEE MTTT*, France, 2002.
- [5] S. Haddad et al., *IEEE Electron Device Lett.*, vol.11, p. 514-516, 1990.