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Fast Speed Bipolar Operation of Ge-Sb-Te Based Phase Change Bridge Devices

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1. Introduction

Phase-change memory (PCM) is one of the most promising candidates for the next generation memory due to its advantages such as high scalability, low process complexity, low cost, and high programming speed. The bridge type devices using GeSb have demonstrated low programming current and high programming speed with a cross-sectional area of only 60 nm^2, indicating the potential for extreme scaling [1]. Similar lateral structures using doped SbTe also showed high programming speed and low current [2,3]. It is notable that both, the Ge-Sb and Sb-Te systems, are growth-dominated materials, while the most commonly used Ge-Sb-Te (GST) PCM material is nucleation-dominated. In addition, it has been reported that the film thickness of GST may affect the crystallization speed [4]. Therefore, the behavior of GST devices with film thicknesses < 10 nm is of great interest. We fabricated doped $Ge_2Sb_2Te_5$ (GST) devices with a film thickness as low as 5 nm. The electrical properties of the devices in different operation modes are described in this paper.

2. Experimental

The bridge devices with doped GST were fabricated on Si wafers by combining Kr-F lithography and e-beam lithography [1]. An SEM picture of a fabricated phase-change bridge device is shown in Fig. 1. The device consists of a doped GST bridge crossing two underlying TiN electrodes. The thickness of the device was kept at 5nm. The width of the device varied from 20 nm to 50 nm.

3. Results

By applying short pulses (30 ns) above 3 V, we can easily RESET the device. On the other hand, the SET resistance as a function of pulse width and amplitude is shown in Fig. 2. It is clear that the RESET-SET transition was difficult to occur by using a short (tens of ns) and low voltage (less than 3 V) SET pulse. The resistance was reduced only when the SET voltage was high and a long pulse width could further reduce the resistance. The high operation voltage and the long pulse width are not desirable for solid-state memory applications.

In order to investigate the full spectrum of the device behavior, we applied negative pulses to the device, which is not the normal PCM operation mode. Fast voltage pulses were used to operate the device. Typical transient SET and RESET voltage and current traces are shown in Fig. 3. The rising time and plateau width were 5 ns and 20 ns, respectively, for both SET and RESET pulses. The fall time of a RESET pulse was 2 ns and that of the SET pulse was 30 ns. The profiles of the RESET and SET pulses were kept the same in this work unless otherwise specified.

Fig. 4 shows the resistance transitions between SET state and RESET state after different programming pulses. For the SET-RESET test, the device was always programmed to the SET state before a RESET pulse, and vice versa. By a positive RESET pulse > 2.8 V, the device switched to RESET. The RESET-SET transition took place when the SET was < -2.2 V. Even though the SET window was not found in the positive voltage region, the significant window between RESET and negative SET revealed the possibility of bipolar operation of these devices, which is very similar to RRAM [5].

In order to clarify if it is a RRAM operation, 4 typical I-V curves are shown in Fig. 5. SET pulses were applied in lines 1, 2, and 3; and a RESET pulse was applied in line 4. The devices in line 2 and line 3 started from a RESET state. The initial resistances were 4.1 M-ohm and 2.4 M-ohm, respectively. During a 2.5V SET pulse, the device showed a clear threshold transition from the OFF state to the ON state near the maximum value of voltage in line 2. The V_{hold} was found at 0.8V. After the SET pulse, the device was still in the RESET state. In line 3, the threshold switching was also found but the V_{hold} was not found, indicating the phase–transition. The final resistance, 16k, also confirmed the phase change. Both line 1 and line 4 are from the SET state (R<20k ohm). Both curves show typical I-V behavior of a SET device. In line 4, after a 3.5 V RESET pulse, the resistance of the device was increased to 0.9 M-ohm. These four curves confirm several facts. (a). The bipolar operation in these devices is a phase change operation, not a RRAM switching. (b). Uni-polar operation is not practical in these devices. (c). Even in the ON state, the resistance of the device is slightly lower than that in the crystalline state. The reason why bipolar operation is more efficient than the unipolar operation is still not very clear. We suspect that the Thomson effect may play an important role in the bipolar operation of the devices. It has been reported that Thomson effect results in asymmetric heating in phase change material and shifts the amorphous region toward the anode of the bridge, as shown in Fig. 6 [3]. The SET operation results in an asymmetric heating in the asymmetric RESET region. In the unipolar operation, the directions of

RESET and SET are the same. As a result, the heating zone is right next to the electrode and results in a low heating efficiency. In contrast, the bipolar operation causes the opposite direction for asymmetric temperature distribution for RESET and SET and results in a more efficient SET operation.

Fig. 7 shows the cycling results and 10k cycles could be obtained on a device with 50 nm width and 5 nm thickness.

3. Conclusions

Bridge type phase change devices were built for GST study. Bipolar operation is sufficient for programming the device in a fast speed while the unipolar operation is slow. Detailed transient characteristics were studied and confirmed that the bipolar operation is a phase change operation. The endurance test shows that the device can be cycled for more than 10k times under bipolar operation.

References

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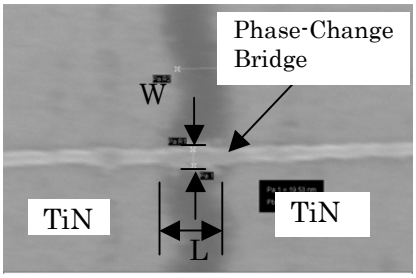

Fig. 1 SEM picture of a thin-film phase-change bridge memory cell, implemented with doped-GST. The length (L) of the bridge is 60nm, and the thickness (t) and width (W) are 5 nm and 20 nm, respectively.

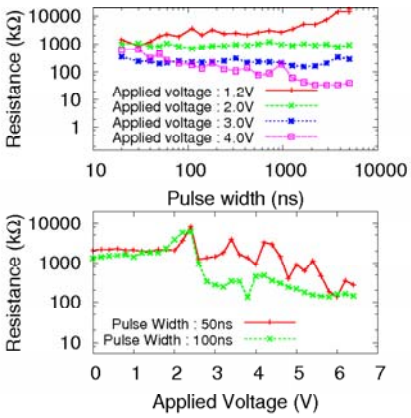

Fig. 2 Measured resistance versus varying plateau width and amplitude of SET pulses in (a) and (b), respectively. In (a), square pulses were applied with varying plateau widths ranging from 20ns to 5μs with various amplitudes of pulses ranging from 1.2V to 4.0V. In (b), the rise and fall time are 5ns and 30ns, respectively, and the pulse widths are 50ns and 100ns. The pulse voltage was varied from 0.0V to 6.4V.

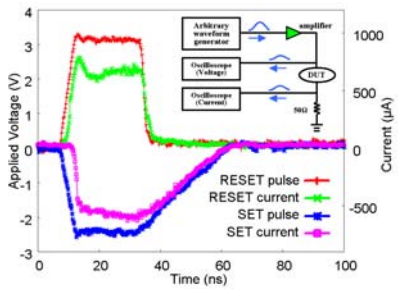

Fig. 3 Transient voltage and current trances for RESET and SET pulses. By careful design of the tester, no significant overshooting and fluctuation was found in the voltage pulses. This insures the possibility of investigation the detailed transient behavior of the devices.

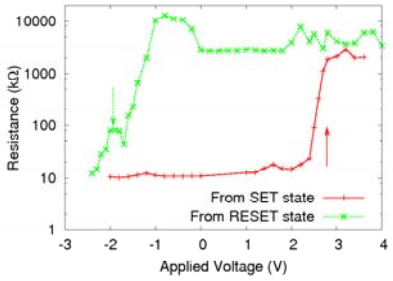

Fig. 4 R-V characteristics for both SET-RESET and RESET-SET transitions. The resistance increases abruptly to the RESET state from the SET state for voltages larger than 2.8V, and SET from RESET when the voltage was lower than -2.2V.

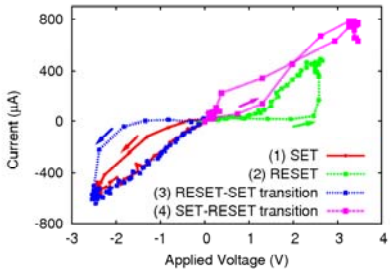

Fig. 5 I-V characteristics of the device under RESET and SET operations.

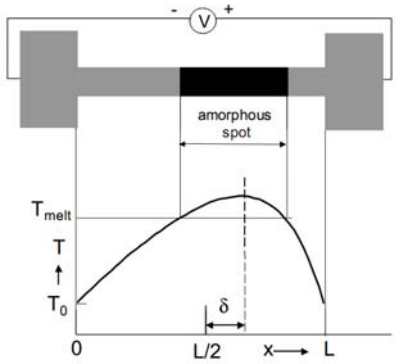

Fig. 6 Asymmetrical temperature distribution along the line, due to the Thomson effect; the amorphous spot is shifted from the middle of line by an amount δ. (Reference 3, Fig. 2.)

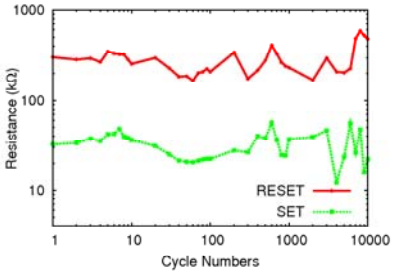

Fig. 7 A typical cycling result of the bridge device. Square shaped SET pulses of 120 ns were used in this case.