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A Dynamic Adaptive Reference Generation Scheme for 1T1C FeRAM

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1. Introduction

The generation of reference signal is important for 1T-1C FeRAM[1]. The structure reported in [1] (Fig.1(a)) fatigus a memory cell and a reference cell at different rates, to overcome this drawback, a 1T-1C memory array where the reference cells are shared among all the cells on the same wordline (Fig.1(b)) is proposed by Joseph and Yadollah[2]. In this method, reference voltage V_{ref} is generated separately for each row of the memory array at the time of data retrieval. This fatigues the reference cells at exactly the same rate as those of the data cells in the same row. To share V_{ref} among the sense amplifiers (SA) of the neighboring columns, V_{ref} is converted into current I_{ref}. It is mirrored locally to each neighboring column and compared with the readout signal by a SA module (including SA, V-I converter, write-back circuit and current mirror). But in this way, the sense margin of the readout signal, defined as the minimum difference between readout signal and reference signal[3], would be very small. Normally the reference voltage is the arithmetical average of readout "0" voltage V_0 and readout "1" voltage V_1. So the maximal sense margin is $(V_1-V_0)/2$, and when it is converted into current, the difference is small, which results in bad tolerance of SA. The amplitude of the sense margin thus affects the reliability of the reading process, the smaller the sense margin amplitude the less reliable the reading operation will be and the slower the data can be read out.

2. Dynamic adaptive reference signal generation

However, if the reference signal is generated in a dynamic way, which means the reference current can be larger when readout signal is "0" and smaller when readout signal is "1", the sense margin can be improved. One way to generate the dynamic adaptive reference signal is shown as Fig.2, adding a feedback NMOS transistor at the reference side of the current sense amplifier to adjust the reference current. During read access, V_x(V_1orV_0) appears on BL, V_1 on RBL and V_0 on /RBL, the voltages are then converted to currents I_x, I_1, and I_0, respectively, by identical PMOS transistors. The static reference current $I_{staticref}$ which is $(I_1 + I_0)/2$ is mirrored with α amplitude to provide I_{mref} to each of the neighboring column sense amplifiers. At the same time the feedback NMOS transistor convert V_x to I_n, which is added to I_{mref} to form the dynamic adptive reference current $I_{dynamicref}$. It is $I_{n1}+I_{mref}$ (smaller than $I_{statref}$) when readout signal is "1", and $I_{n0}+I_{mref}$ (larger than $I_{statref}$) when readout signal is "0". Once the currents are set up, the sense amplifiers for all columns are turned on and the currents I_x and $I_{dynamicref}$ compete to pull down their corresponding nodes, sen and senb. The side with smaller current will regenerate to VDD, forcing the other side to GND.

3. Simulation and Discussion

The proposed sensing scheme is implemented in a prototype with a 1k-bit FeRAM in a 0.35 μm process. Fig.3 shows the sense margin of the proposed scheme and the static reference structure in a read cycle. It can be seen that the sense margin of proposed scheme is 9.16μA, which is nearly 3.5 times as the conventional(2.65μA). How large can the sense margin be depends on three important coefficients α, β and γ, defined as follows.

$$I_{mref} = \alpha \cdot I_{statref}, \alpha < 1 \quad (1)$$

$$I_{n0} = \beta \cdot I_{n1}, \beta < 1 \quad (2)$$

$$I_0 = \gamma \cdot I_1, \gamma > 1 \quad (3)$$

It is noticed that there is current flowing through the feedback NMOS transistor no matter the BL is "0" or "1" , so Formula.4 must be satisfied to make the sense margin of "1"and "0" are the same.

$$I_{\text{ref}} = I_{mref} + (I_{n0} + I_{n1})/2 \quad (4)$$

In this way the sense margin of readout signal is shown in Formula.5, while it is $(\gamma-1)I_1/2$, if the reference current is generated in a static way.

$$\begin{aligned} \text{SenseMargin} &= (I_{mref} + I_{n1}) - I_1 \\ &= \frac{I_0 - I_1}{2} + \frac{I_{n1} - I_{n0}}{2} \\ &= \frac{(\gamma-1)I_1}{2} + \frac{(1-\beta)(1+\gamma)}{2(\beta+1)} I_1 \cdot (1-\alpha) \end{aligned} \quad (5)$$

It is obvious that the sense margin can be adjusted by α, β and γ. Unfortunately, β and γ is decided by the process character, and can't be changed. Then it means that there is liner relationship between α and sense margin (smaller α gets larger sense margin). And α can be set by adjusting the W/L of the feedback NMOS transistor. But considering the layout of SA must be suitable for the memory array, the W/L of the feedback NMOS transistor can't be larger than 15 in general. So the smallest α in the proposed scheme is 6/7 to reach the largest sense margin of 9.16μA (245% larger than conventional structure). Because of the larger

sense margin, the proposed scheme achieves a 14.5% reduction in actual sensing to previous work, as shown in Fig.4. All the benefits above are got by adding an feedback NMOS transistor, which increases the area of SA circuit module by only 19.5% as overhead (Table.I).

4. Conclusion

A 1T-1C FeRAM reference generation scheme which can provide dynamic adaptive reference current based on bitline voltage is achieved by adding a feedback NMOS transistor at the reference side of the sense amplifier. The proposed scheme increases the sense margin of the readout current by 245% and reduces the actual sensing time by 14.5%, at the expense of relatively small additional area.

Acknowledgements

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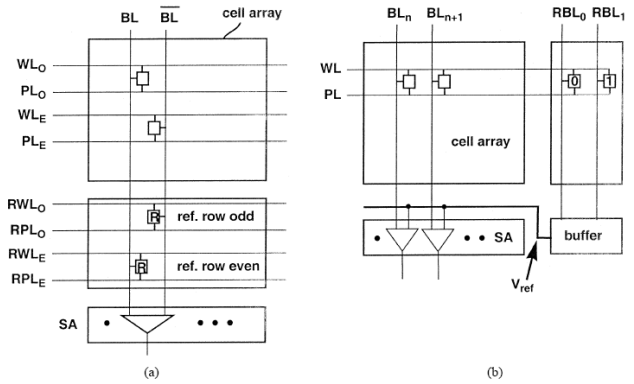

Fig.1 Reference generation schemes. (a) Sharing reference cells among cells in a column. (b) Sharing reference cells among cells in a row.

Table I Scheme Characters

	conventional	proposed	improvement
sense margin	2.65μA	9.16μA	245%
sensing time	6.9ns	5.9ns	14.5%
area*	9.43μm^2	11.27μm^2	-19.5%

*the area of SA circuit module

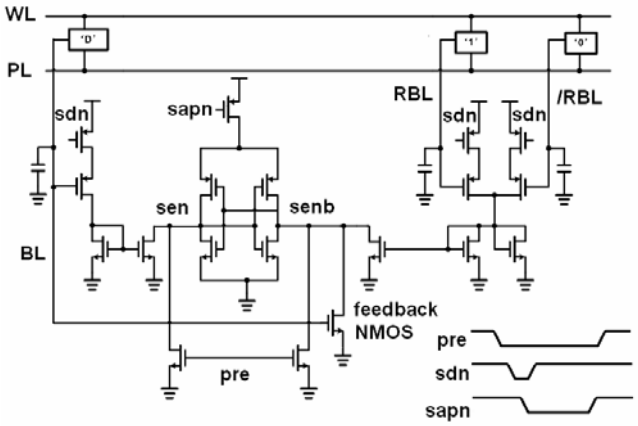

Fig.2 Dynamic adaptive reference generation scheme for 1T-1C FeRAM

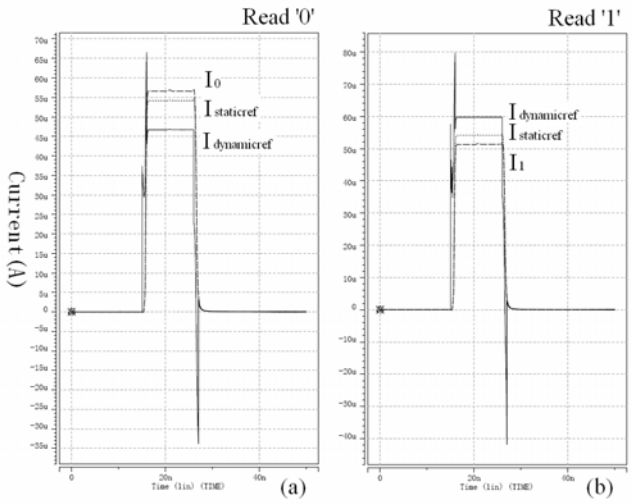

Fig.3 Sense margin of the proposed scheme and the static reference structure. (a) Reading stored ’0’. (b) Reading stored ’1’.

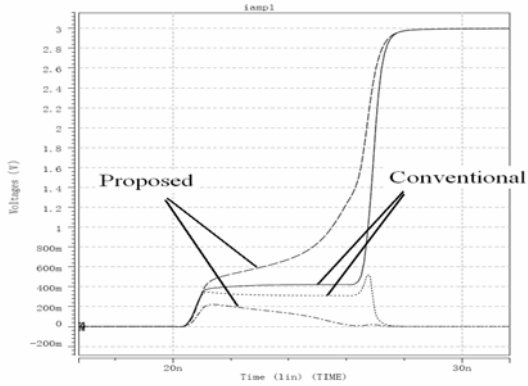

Fig.4 Readout Voltage of proposed and conventional scheme.