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Writing Disturbance-Free of a Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode

Susumu Horita and Bui Nguyen Quoc Trinh

Japan Advanced Institute of Science and Technology (JAIST)
1-1 Asahidai, Nomi, Ishikawa 923-1292, Japan
Phone: (+81)-0761-51-1564 E-mail: horita@jaist.ac.jp

1. Introduction

Ferroelectric gate field-effect transistor memory (F-FET) is well known as one of the ultimate nonvolatile memories because of its remarkable features such as non-destructive readout, high packing density, high reading speed, low power consumption and so on. Therefore, considerable researches have been carried out on F-FET [1,2]. However, F-FET has not been commercialized so far due to the serious problems such as short retention time and high writing voltage. In order to overcome these problems, a new F-FET memory (denoted as IF-FET) has been proposed, in which an intermediate electrode (I.E.) for data-writing is inserted between the ferroelectric gate and the buffer layer [3,4]. Recently, we have proposed an improved operation method for data-writing and –reading of IF-FET. In this method, we use a memory state of Pr^0 which is non-polarized in the ferroelectric capacitor. Also, for data-reading, following a positive reading voltage V_R^+, a negative reading voltage V_R^- is applied to return the readout memory state to the initial one. By using this operation, the readout endurance reached more than 10^8 reading cycles, and the retention time exceeded about 10 years [5]. However, in the case of memory array structure in an integrated circuit, the data disturbance in writing operation (writing disturbance) is caused seriously. In this conference, we propose a new writing operation for writing disturbance-free and verify it adequate experimentally.

2. Fundamental Operation

Figure 1 (a) shows a schematic equivalent circuit of the IF-FET memory, which consists of a ferroelectric capacitor C_f connected serially to an n-channel reading-MOSFET (R-MOSFET). The output voltage V_O is measured on a resistor R at the drain biased by V_D. We use the two kinds of memory states, positive remanent polarization Pr^+ and roughly non-polarization Pr^0. Figure 1 (b) shows P-E hysteresis loop of C_f, where C_{fl} and C_{fh} are denoted as ferroelectric capacitances near the Pr^+ state and the Pr^0 state, respectively, in the positive electric field E. Because C_f is proportional to the gradient $\Delta P/\Delta E$ of the P-E slop, C_{fh} of Pr^0 is much larger than C_{fl} of Pr^+. The fundamental operation is as follows; Pr^+ state is produced by direct application of two positive pulses to the C_f, and Pr^0 state is produced by two combined pulses of a positive pulse V_W^+ followed by a negative pulse V_W^- as shown in Fig. 1. The V_W^+ is to reset the previous stored memory state and the V_W^- is to determine the polarization of Pr^0. The reading pulse consists of a positive voltage V_R^+ followed by a negative voltage V_R^-. Because the I.E. voltage V_I of Pr^+ sate is lower than V_I of Pr^0 state due to the large capacitance ratio of C_{fh}/C_{fl}, I_D in Pr^+ is much smaller than that of Pr^0 state. So, we can distinguish the memory state by measuring the difference in V_O between Pr^+ and Pr^0 states.

Fig. 1(c) shows a typical nondestructive readout characteristics for Pr^0 state, using the reading pulse heights of V_R^+ = 3.5 V and V_R^- = -2.0 V. The V_O was measured in turn from the first to the tenth readout with retention time of 1 min after each readout. The reading pulse has two periods per one readout operation. Since V_O for each readout shows the almost same response, it can be said that IF-FET memory behaves good nondestructive readout.

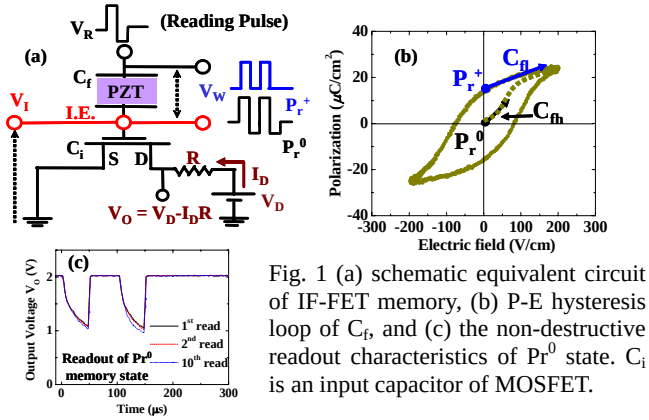

Fig. 1 (a) schematic equivalent circuit of IF-FET memory, (b) P-E hysteresis loop of C_f, and (c) the non-destructive readout characteristics of Pr^0 state. C_i is an input capacitor of MOSFET.

3. Improvement Principle for Writing Disturbance

Figure 2 shows a schematic array of IF-FET memory cells in an integrated circuit. In this figure, an additional writing MOSFET (W-MOSFET) is used as a switch to short-circuit R-MOSFET to the ground for data-writing. Setting the bitline B_{11} high and applying the writing pulses of Pr^+ and Pr^0 through the worldline W_1 and W_2, respectively, then, the C_{11} and C_{21} cells store Pr^+ and Pr^0 memory states, respectively. By this programming, the non-selected cells with the ground bit lines, e.g., C_{12} and C_{22}, are also applied by the writing pulses of Pr^+ and Pr^0, respectively. Not full but partial voltages of the writing pulses drop on the C_f of C_{12} and C_{22}. If the C_f of C_{12} is Pr^0 sate, it changes toward Pr^+ state due to Pr^+-writing, which means writing disturbance occurs in the C_{12} cell. On the other hand, if the writing pulse is Pr^0, any stored memory state remains, which means that Pr^0-writing is disturbance-free. This is because the form of the Pr^0-writing pulse is similar to that of the non-destructive reading pulse.

In order to improve disturbance due to Pr^+-writing, we propose a new writing operation, in which Pr^0-writing pulse is used to write Pr^+ memory state as shown in Fig. 3.

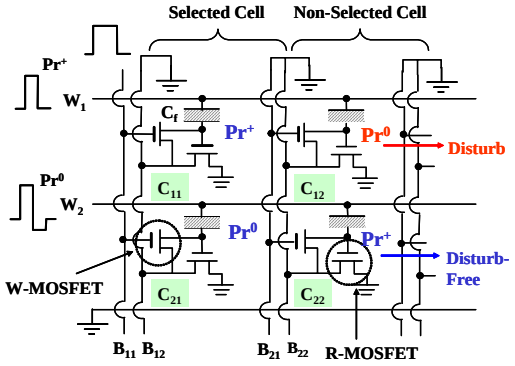

Fig. 2 Previous writing operation for integrated array of IF-FET memory cells.

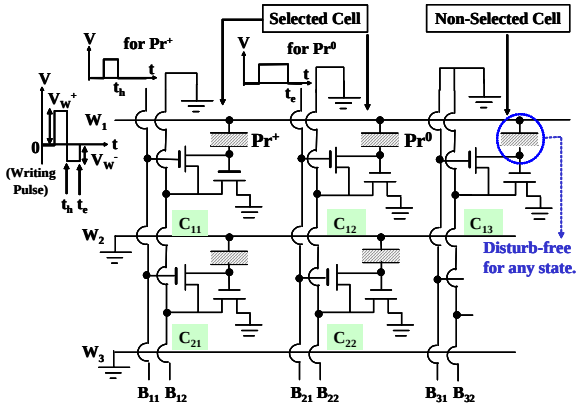

Fig. 3 New writing operation for integrated array of IF-FET memory cells. It serves writing disturbance-free.

The writing operation is performed by controlling the timing of the bitline voltage. For instance, when the voltage of the B_{11} line is fallen down to the ground before the Pr^0-writing pulse changes from positive V_W^+ to negative V_W^- at t_h, the C_{11} cell can be stored as Pr^+ state. This is because the positive voltage of V_W^+ drops on only C_f but V_W^- drops on both C_f and C_i of MOSFET. Since the voltage drop on both C_f and C_i is the same bias condition as the nondestructive readout, the Pr^+ memory state written by V_W^+ can remain in the C_{11} cell even after V_W^- application. On the other hand, for the C_{12} cell, the voltage of the B_{21} line is not fallen down to the ground till the whole writing pulse is finished at t_e. By this operation, the memory state of the C_{12} cell is written as Pr^0. Because the waveform of the writing pulse is the same as the nondestructive reading pulse, writing disturbance of any non-selected memory cell becomes free.

4. Experimental

For the sake of simulation of writing disturbance in the new writing operation, we performed the following measurement sequence, using a discrete circuit as shown in Fig. 1(a). Pr^+ or Pr^0 state was written into C_f and the writing pulse of Pr^0 is applied to the stored memory between the top electrode and the ground, floating the I.E. electrically. The number of writing times was varied from 10^0 to 10^8. After the disturbance, we measured the output voltage V_O of each stored memory state. In this case, the sample structure of C_f consisted of (RuO_x top electrod)/PZT/Pt/RuO_x bottom electrode) on the SiO_2/Si substrate. The details are mentioned elsewhere[4]. The pulse heights of V_W^+ = 4.0 V, V_W^- = -2.3 V, V_R^+ = 3.5 V, and V_R^- = -2.0 V. The MOSFET was a commercial of 2SK679A with C_i = 180 pF.

5. Results and Discussion

Figure 4(a) shows the writing disturbance characteristics of Pr^0 memory state in the previous writing operation. V_O of the Pr^0 memory state disturbed by Pr^+-writing pulse is quickly increased with the writing time, which indicates serious writing disturbance. Because the stored Pr^0 state was continuously applied by the positive writing pulses, it was changed toward a positive polarization. Figure 4(b) shows the disturbance characteristics of Pr^+ and Pr^0 stored memory states in the new writing operation using Pr^0-writing pulse. From this figure, it is found that writing disturbance is achieved free for any stored memory sate. However, the V_O of the both memory sates are slightly decreased with the writing time. The application of writing voltage (writing disturbance) to the non-selected cells is repeated many times continuously, which is different from the writing operation with one time. Therefore, the polarization of the stored state is gradually changed from the initial state to the steady state with less positive or more negative. These disturbance levels are supposed to be negligible for actual memory operation, and they can be reduced by optimization of writing operation condition, ferroelectric material and memory circuit. So, it can be concluded that the new writing operation is effective for writing disturbance-free in IF-FET memory.

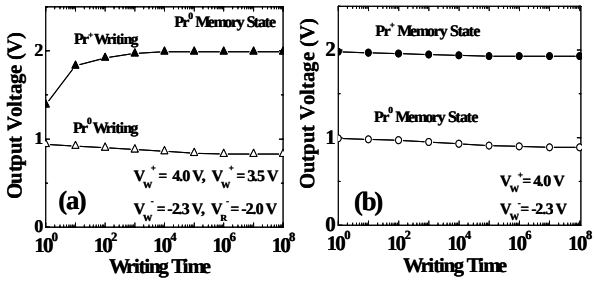

Fig. 4 Disturbance characteristics of (a) Pr^0 states under the previous Pr^+- and Pr^0-writing operations, and (b) Pr^+ and Pr^0 states under the new writing operation.

6. Conclusion

By using the new writing operation, writing disturbance-free can be achieved for any memory state in IF-FET memory until at least 10^8 writing times.

References

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